



# **“Fixed Frequency Oscillator” Novel Approach to Transceiver Architecture Design**

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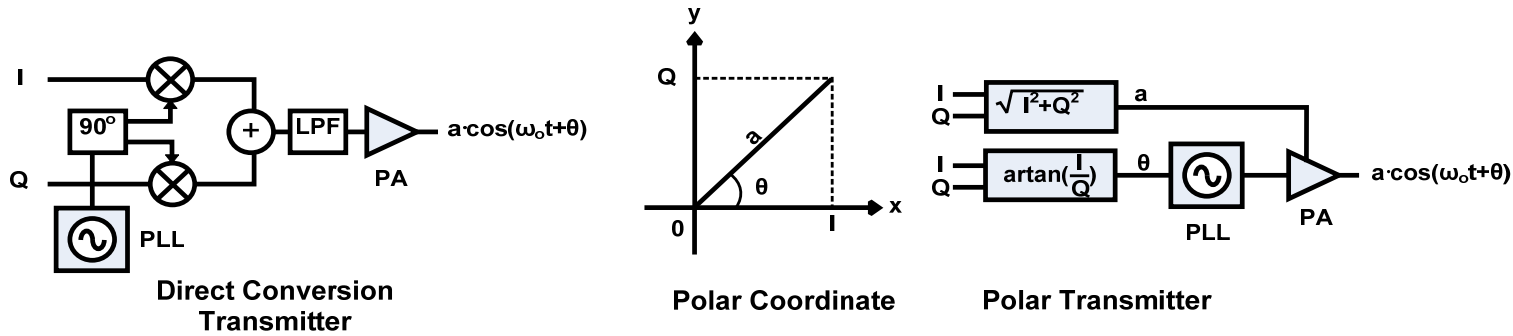
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# Local Oscillator Generation in Transceivers

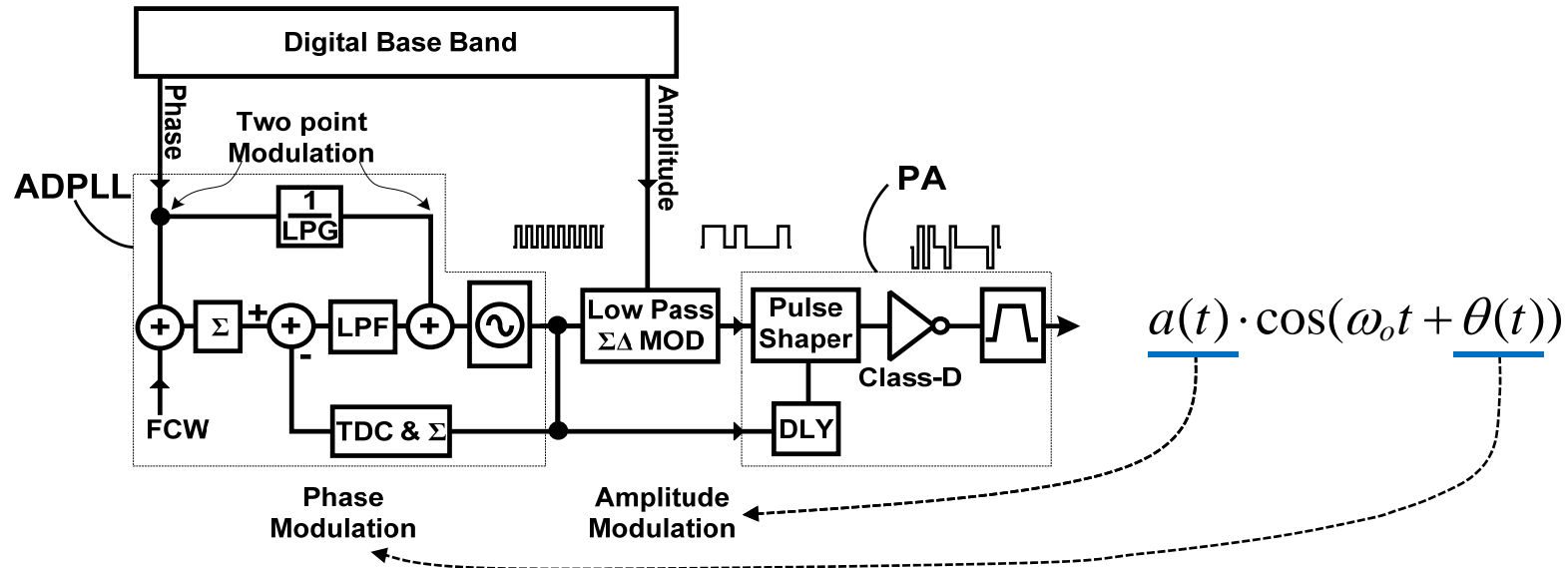


- ▶ Over the years, the Phase Lock Loop (PLL) frequency synthesizer has become ubiquitous to transceiver design
- ▶ Its primary role is local oscillator (LO) generation for up/down conversion of signals to/from antenna/baseband
- ▶ Advanced communication systems have stringent requirements on phase noise, jitter, reference breakthrough, tuning speed and tuning resolution that are contradictory parameters in system optimization
- ▶ Typically, Fractional-N and/or All-Digital PLL implementations are used to address the above
- ▶ In some transmitters, the PLL is used as modulator (polar modulation) instead, bringing additional complication to the design
- ▶ Receivers and Transmitters often suffer from spurious signals generated by these complex PLL synthesizers
  - Fractional spurs, reference breakthrough, etc.

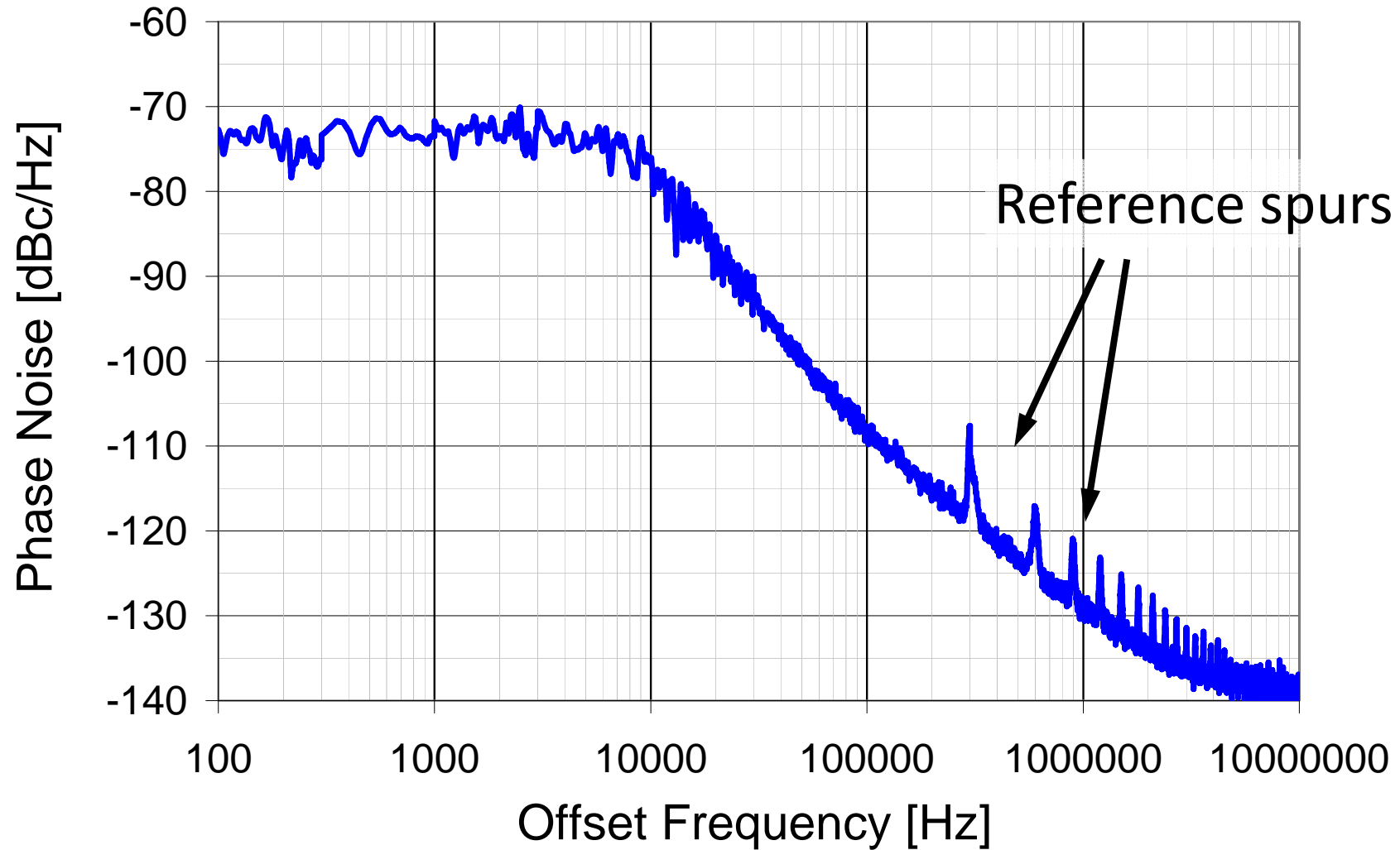
# All-Digital Polar Transmitter



- Digital Polar Transmitter



# PLL Noise and Spurious Example



# Coexistence/Cohabitation of Transceivers



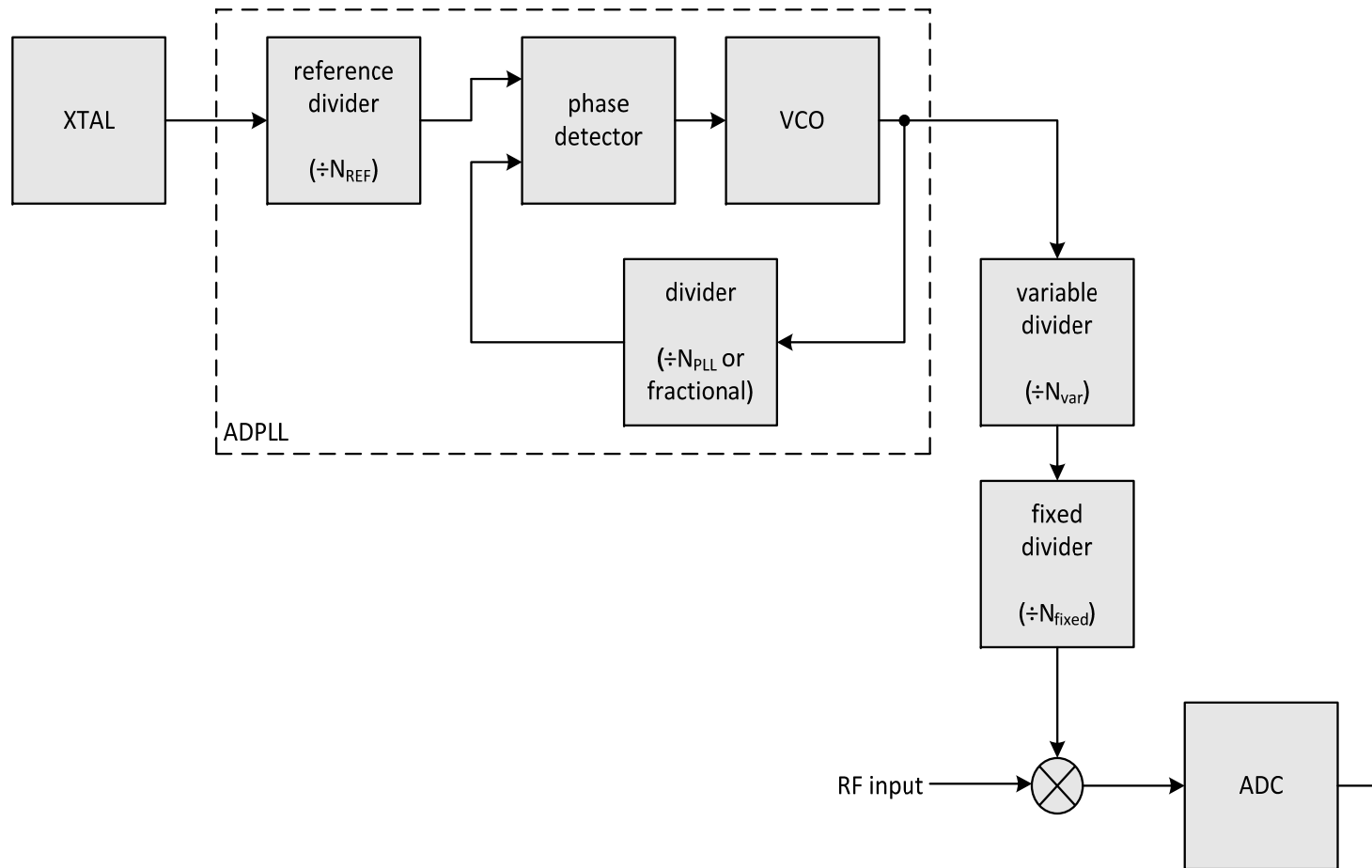
- ▶ High attachment rate of wireless connectivity to mobile handsets spurred the development of connectivity combo devices
  - FM TRx, GNSS Rx, BT/BTLE TRx, WiFi TRx, NFC, all on one chip
- ▶ Internet of Things (IoT) is now setting this trend through to all other devices: Wearables, Smart Watches, Sensors, ...
- ▶ As a consequence, we find multiple transceivers in close proximity (on the same chip) operating concurrently
- ▶ Isolation between, in particular, the oscillators of these transceivers poses a serious challenge – magnetic, capacitive and supply coupling
- ▶ In a typical transceiver, LO generation circuits consume a large percentage of the power budget – high frequency and low noise requirements
- ▶ Concurrent operation is often also a power dissipation challenge

# Fresh Look at LO Generation



- ▶ To address today's problems of system complexity, performance, power dissipation and concurrency, we need to revisit the LO generation scheme
- ▶ Making use of modern CMOS process capabilities – high speed and digital signal processing – to simplify system requirements
- ▶ Basic elements of LO generation: PLL, Variable Divider, Fixed Divider
- ▶ PLL frequency and parameters optimized to system requirements and integration capabilities (e.g.: inductor quality factor, process speed)
- ▶ Variable Divider settings and range are potential degrees of freedom
- ▶ Fixed Divider is often used to generate quadrature LO signals ( $/2$ ), ( $/4$ ) and/or harmonic suppression ( $/8$ )
- ▶ Observation: important relation between PLL frequency, Variable Divider, Fixed Divider and ADC (or DAC) bandwidth in Rx (or Tx) path

# Typical LO Generation Scheme in a Receiver



# Frequency Planning Example for FM Radio



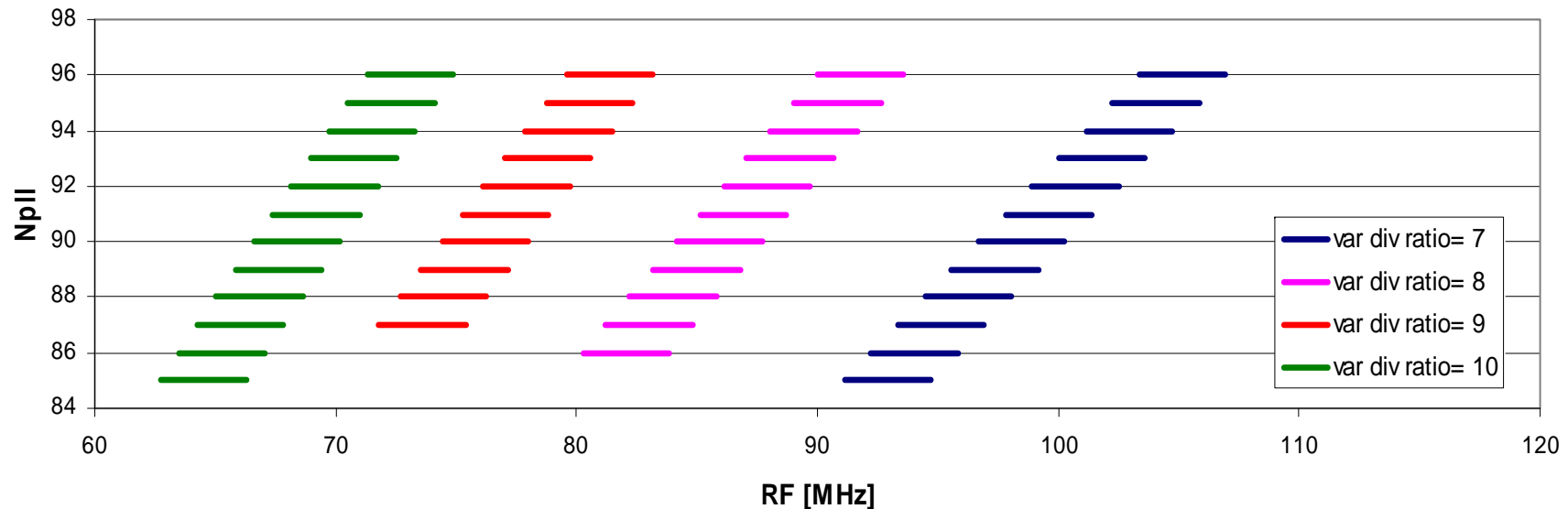
integer N	VCO frequency	LO frequency
96	5990,400 MHz	106,971 MHz
95	5928,000 MHz	105,857 MHz
94	5865,600 MHz	104,743 MHz
93	5803,200 MHz	103,629 MHz
92	5740,800 MHz	102,514 MHz
91	5678,400 MHz	101,400 MHz
90	5616,000 MHz	100,286 MHz
89	5553,600 MHz	99,171 MHz
88	5491,200 MHz	98,057 MHz
87	5428,800 MHz	96,943 MHz
86	5366,400 MHz	95,829 MHz
85	5304,000 MHz	94,714 MHz
84	5241,600 MHz	93,600 MHz

$$f_{VCO,max} = 6 \text{ GHz}; N_{var} = 7; N_{fixed} = 8$$



# Frequency as Function of Divider Ratios

ADC BW = +/- 1.8MHz and Integer-N PLL



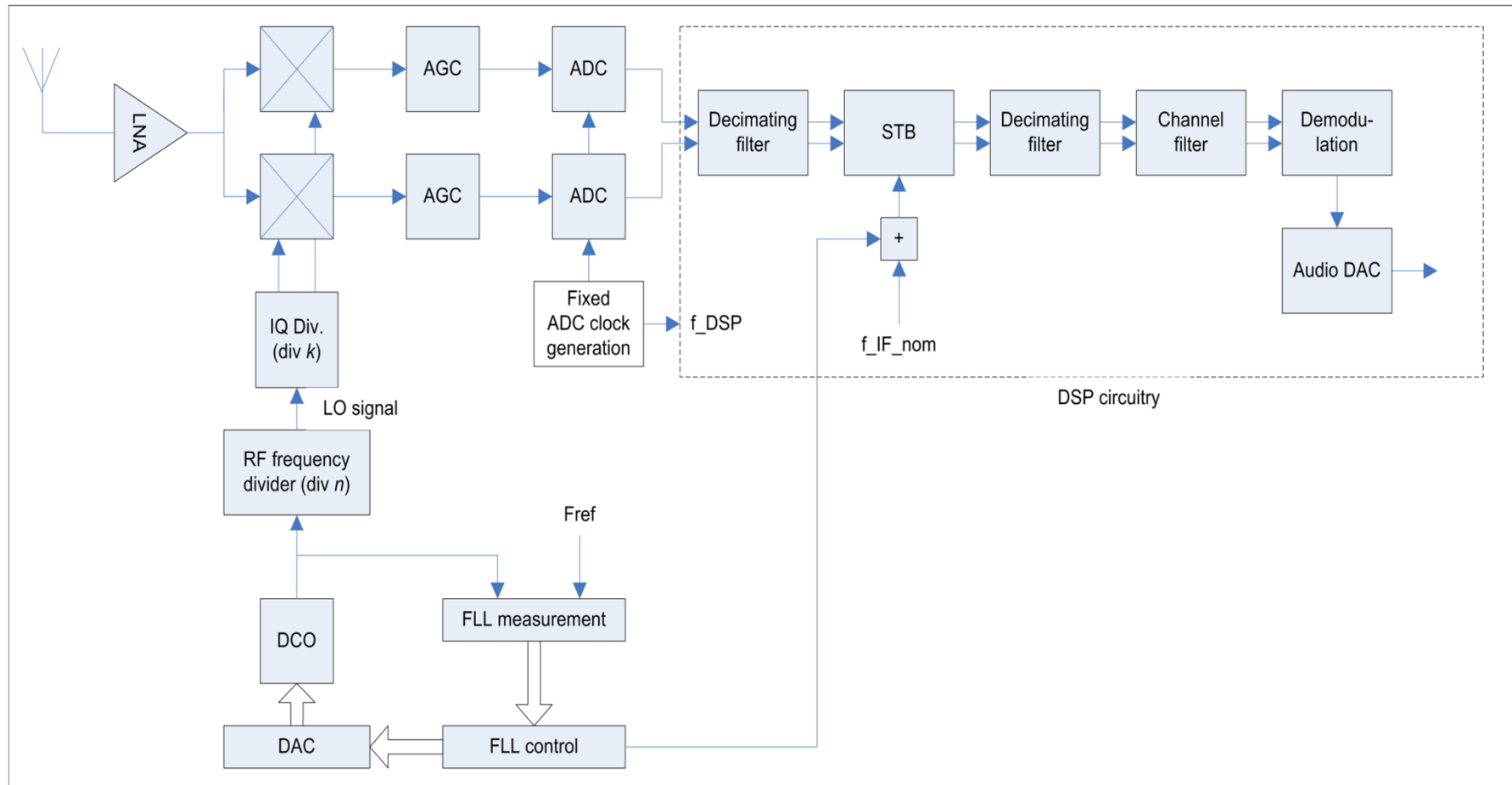
- ▶ Every frequency in a sub-band can be reached by at least 2 different division ratios in the LO generation path
- ▶ Widening the ADC bandwidth increases overlap of sub-bands and consequently narrower PLL frequency range is required

# Fixed-Frequency LO Generation

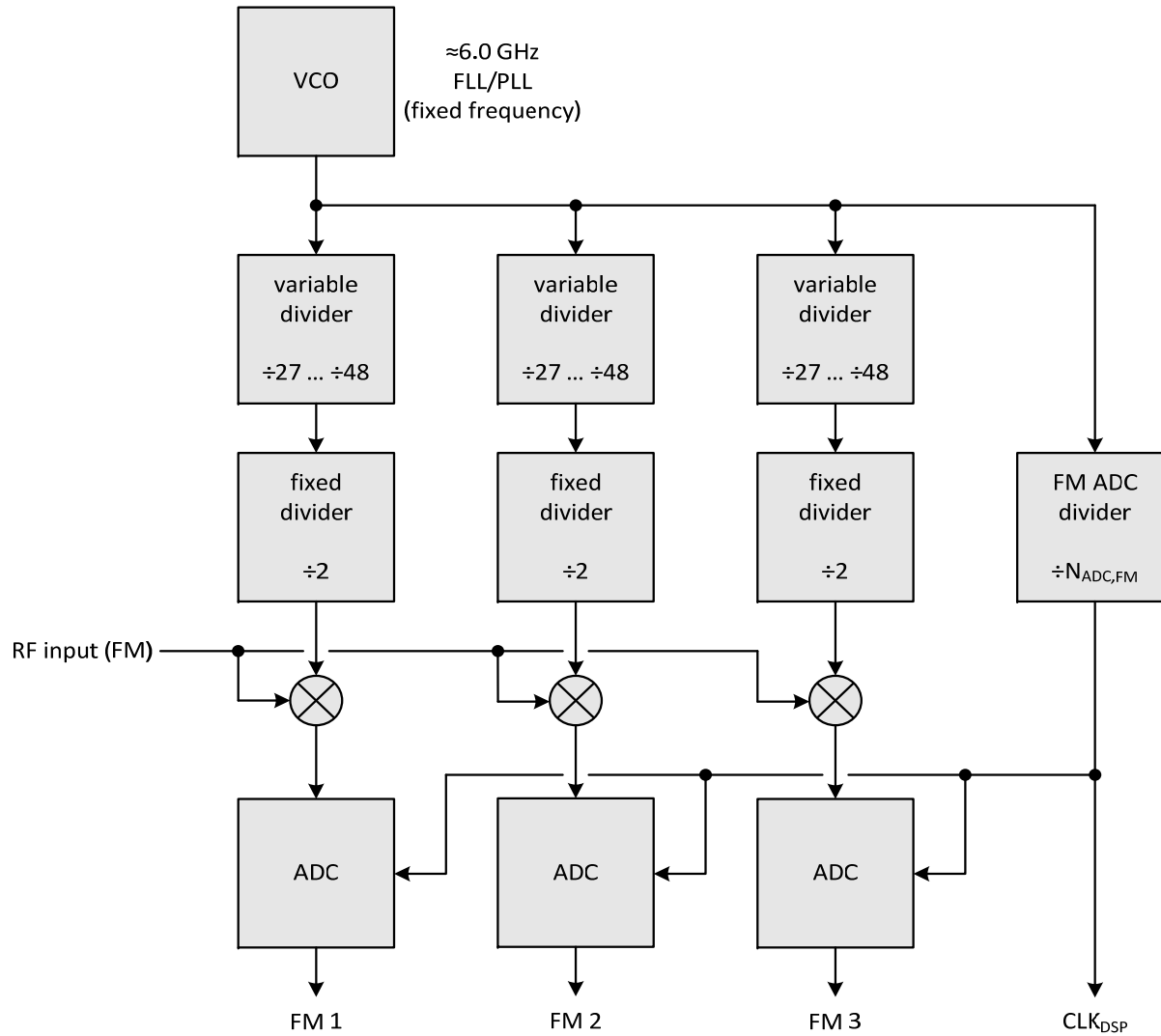


- ▶ As the ADC bandwidth gets wider, there are more options to generate required LO signals – overlapping frequency sub-bands
- ▶ With specific divider/ADC configurations, all required LO signals can be generated purely by Variable Divider settings – only one frequency at PLL oscillator
- ▶ FM receiver example:
  - ▶ PLL frequency = 6GHz, Variable Divider = /27-48, Fixed Divider = /2, ADC bandwidth  $\geq$  5.4MHz
  - ▶ Channel selection by Variable Divider setting in LO (sub-band selection) and “Shift To Baseband” operation in digital domain (fine tuning)
- ▶ Multiple FM receivers operating (concurrently) from one fixed-frequency oscillator for the tuning PLL (and potentially one LNA)
- ▶ AM receiver can be included (wideband, no LO required)

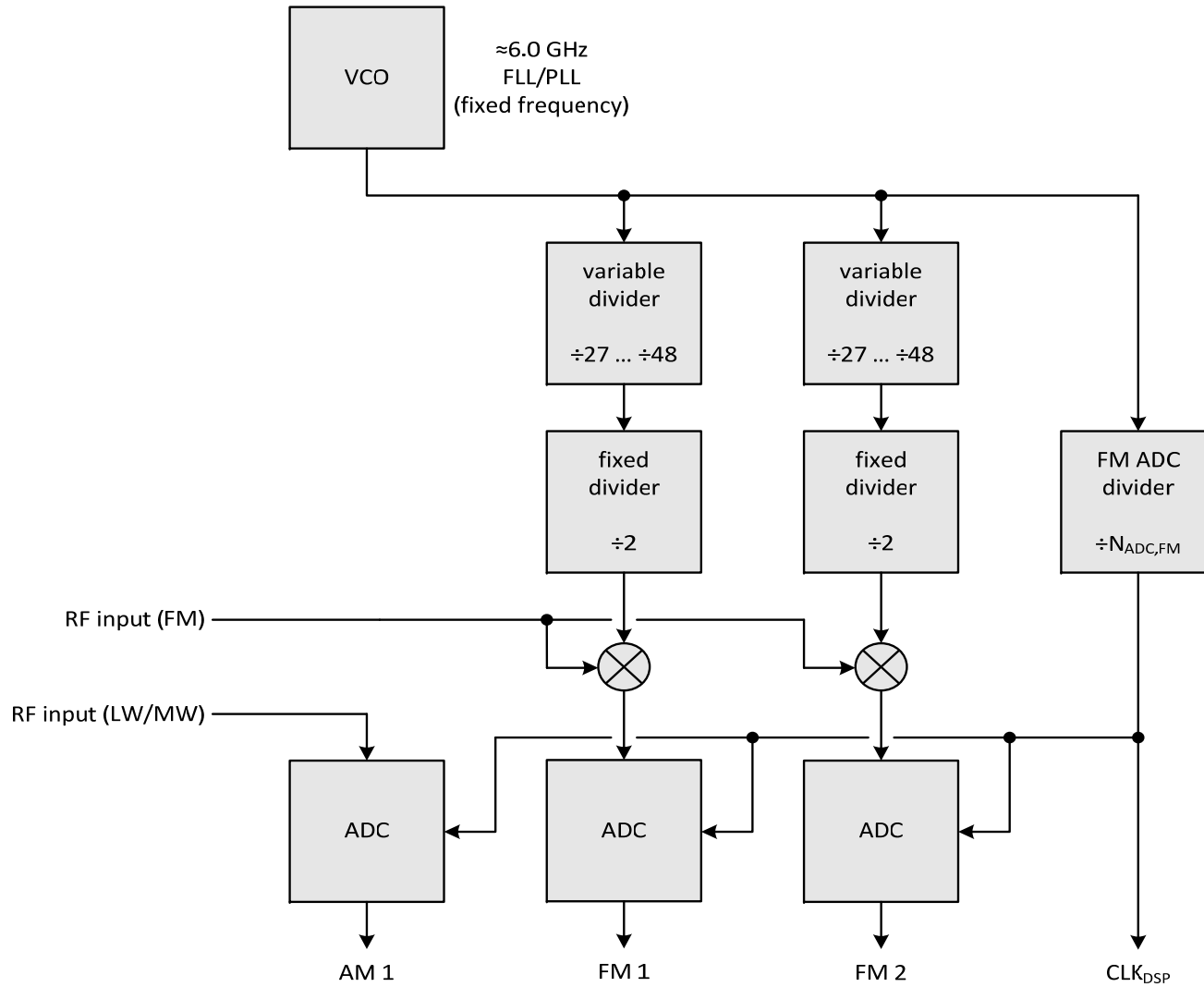
# Coarse/Fine Frequency Tuning in Low-IF Receiver



# Multiple FM Receivers Using One Oscillator



# Dual FM + AM Receivers Using One Oscillator



# Benefits of Fixed-Frequency LO Generation



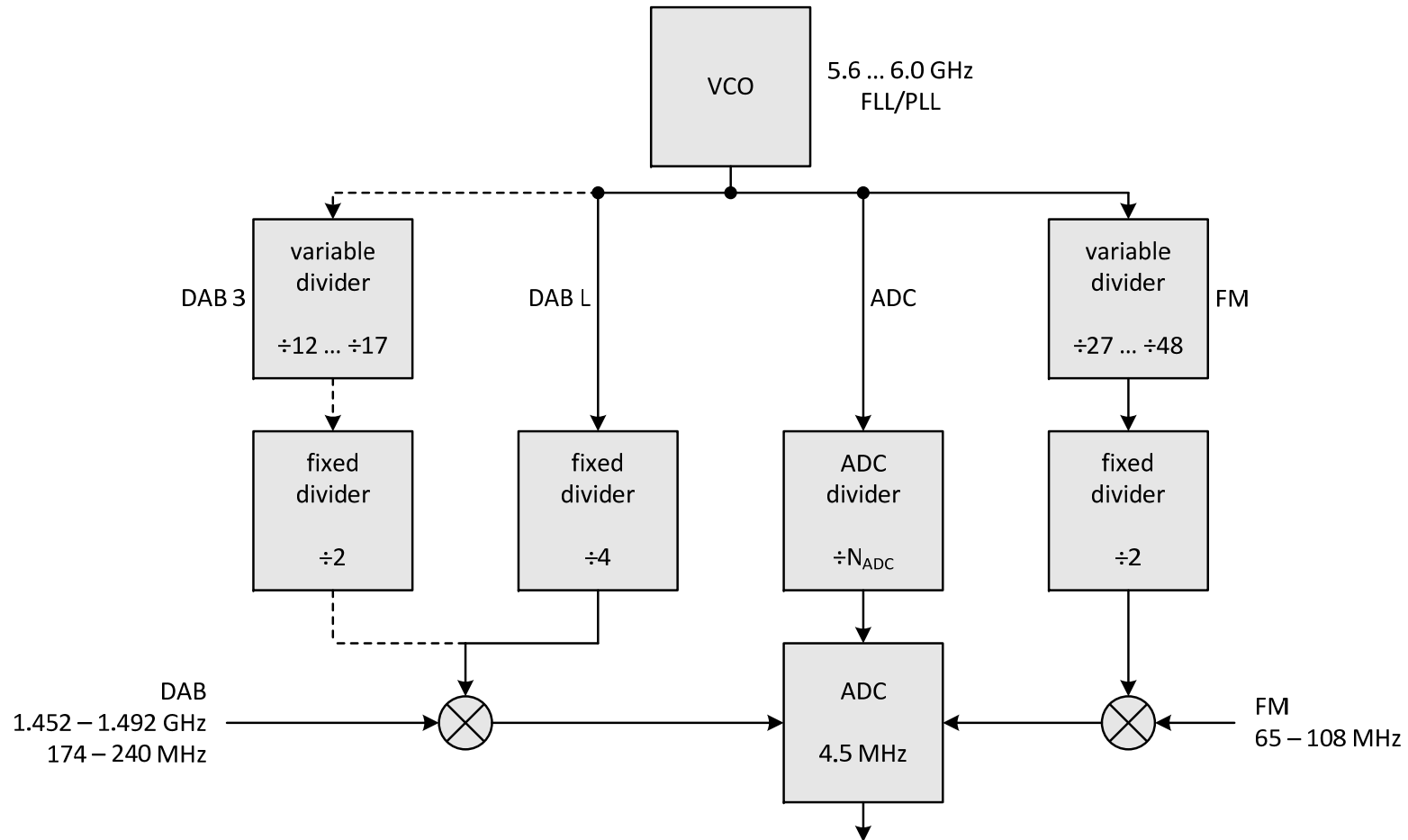
- ▶ Simplification of PLL tuning requirements
  - ▶ Tuning range only to cover process spread
  - ▶ No tuning step resolution requirements
  - ▶ Tuning speed set by dividers (ultra-fast)
- ▶ No fractional spurs
- ▶ Reduced chip area – simpler PLL design used only once in system
- ▶ Reduced power dissipation for concurrent operation
  - ▶ Separate divider chains tune independently multiple receivers
- ▶ ADC/DAC and baseband clocks generated from fixed-oscillator without the need for separate PLL
- ▶ Cohabitation/Coexistence “friendly”
  - ▶ No pulling between oscillators, more frequency planning freedom

# Extension to Other Standards



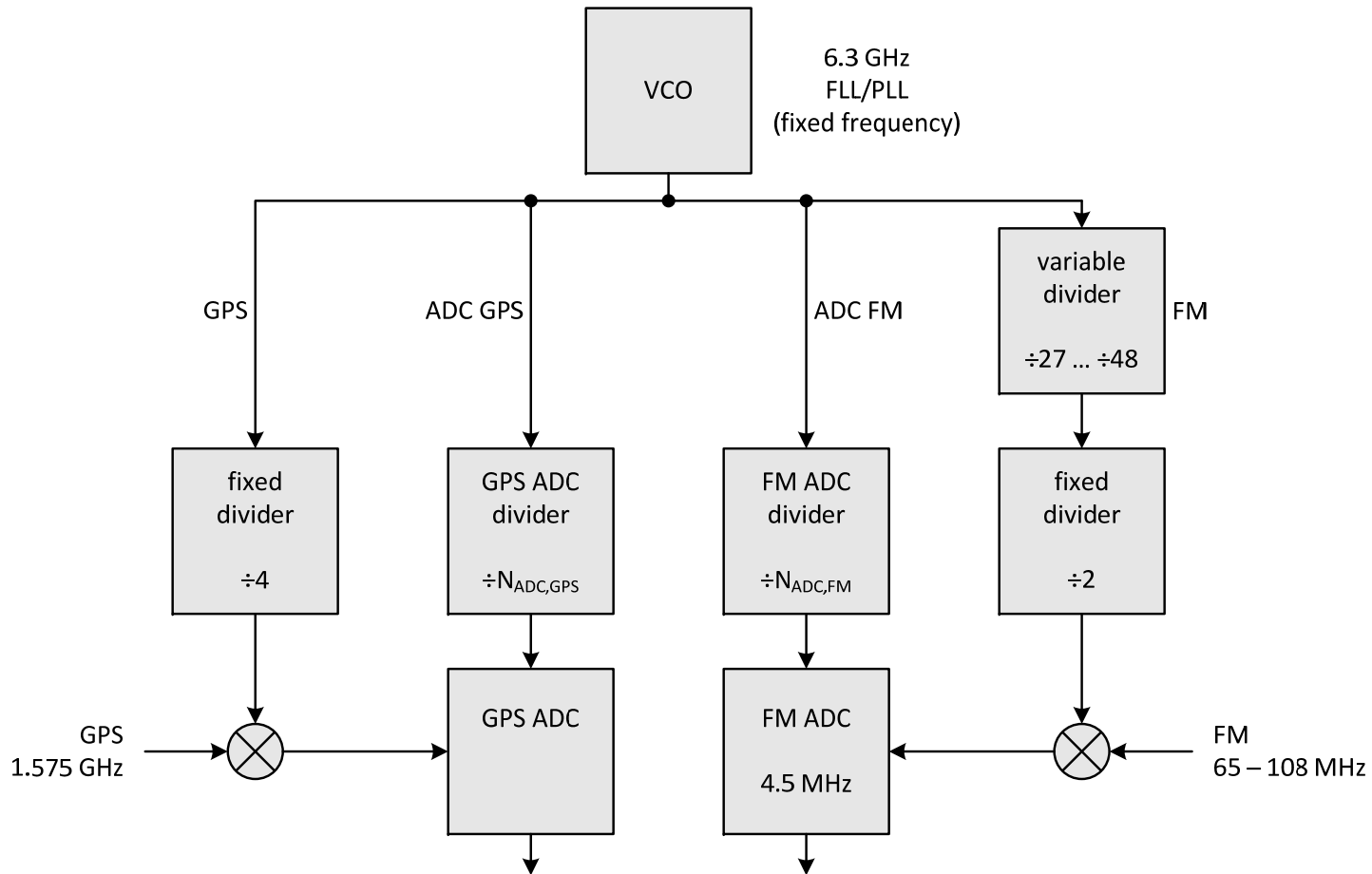
- ▶ The fixed-oscillator concept can also be applied to transmitters
- ▶ Application to other wireless standards requires re-optimization of the system configuration with respect to: oscillator frequency, variable divider, fixed divider and ADC (DAC) bandwidth
- ▶ Standards with higher RF frequencies are more challenging (less degrees of freedom on the variable divider), requiring higher oscillator frequencies and/or wider ADC bandwidths
- ▶ Examples for FM/DAB and FM/GPS combinations
- ▶ FM/DAB combination can be particularly attractive for FM/DAB blending that required concurrent operation of the 2 standards
- ▶ For narrower ADC bandwidths, it is possible to use multiple oscillator settings for DAB, while FM receiver follows by appropriate divider setting
- ▶ Patent: US 8,503,507 B2

# FM/DAB Reception Using One Oscillator





# FM/GPS Receivers Using One Oscillator



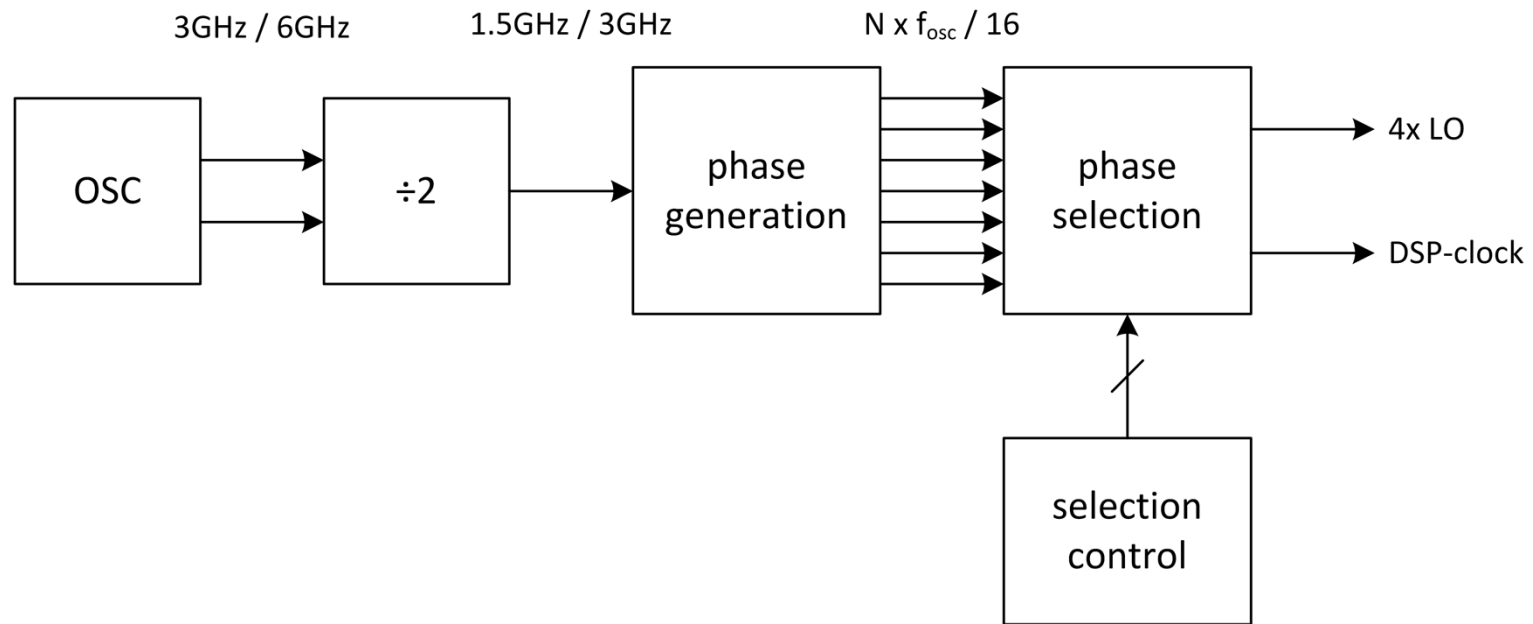


# Multi-Modulus Divider

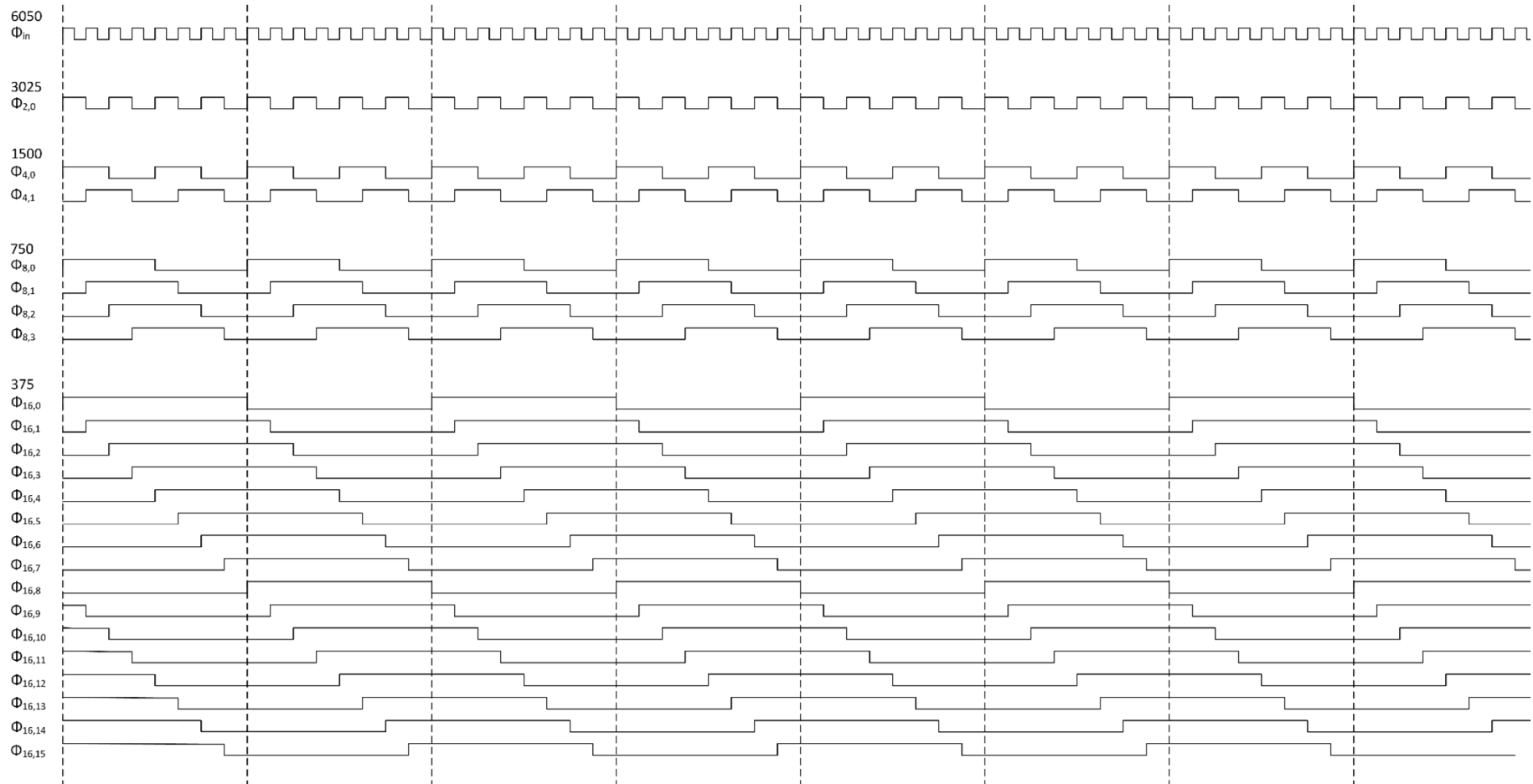
## Opportunities and Challenges

- Frequency divider architecture has a direct impact on the degrees of freedom in system design
- Fixed dividers are used primarily for quadrature LO signal generation and/or harmonic suppression – eat away flexibility in division ratios
  - Even divider ratios: /2, /4 or /8
  - /2 quadrature signals sensitive to oscillator duty cycle
  - /4 quadrature signals insensitive to oscillator duty cycle
  - /8 generating LO waveforms for 3<sup>rd</sup> and 5<sup>th</sup> harmonic suppression
- Merging of variable and fixed dividers and yet delivering required quadrature LO signals increases system design freedom, but needs innovative approach
  - This means arbitrary (odd and even) divider ratios 27, 28, 29, ..., 47, 48
  - Yet maintaining high frequency, phase accuracy, duty cycle control and low noise requirements

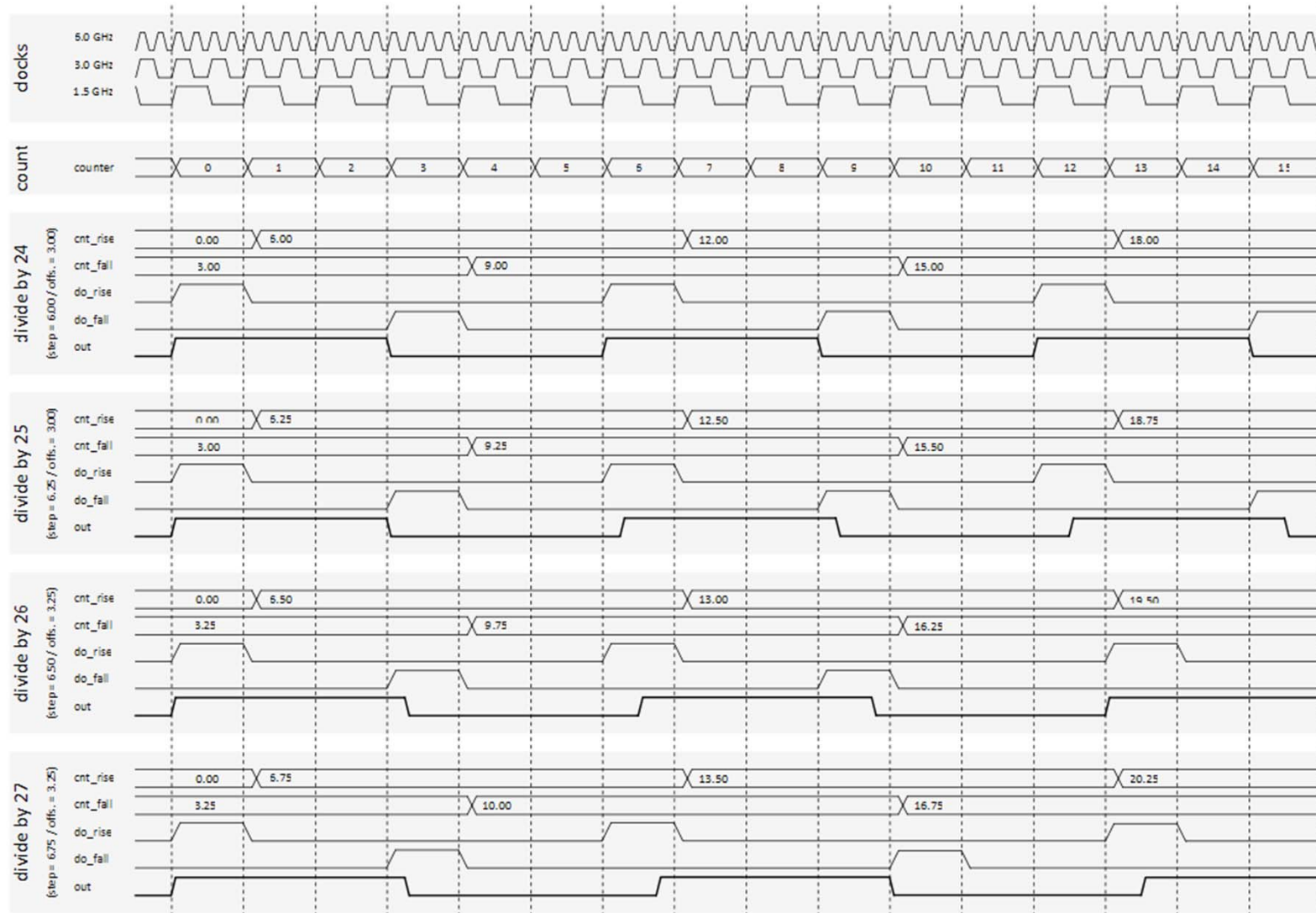
# Phase-Shifter Divider Concept



# Phase-Shifter Waveforms



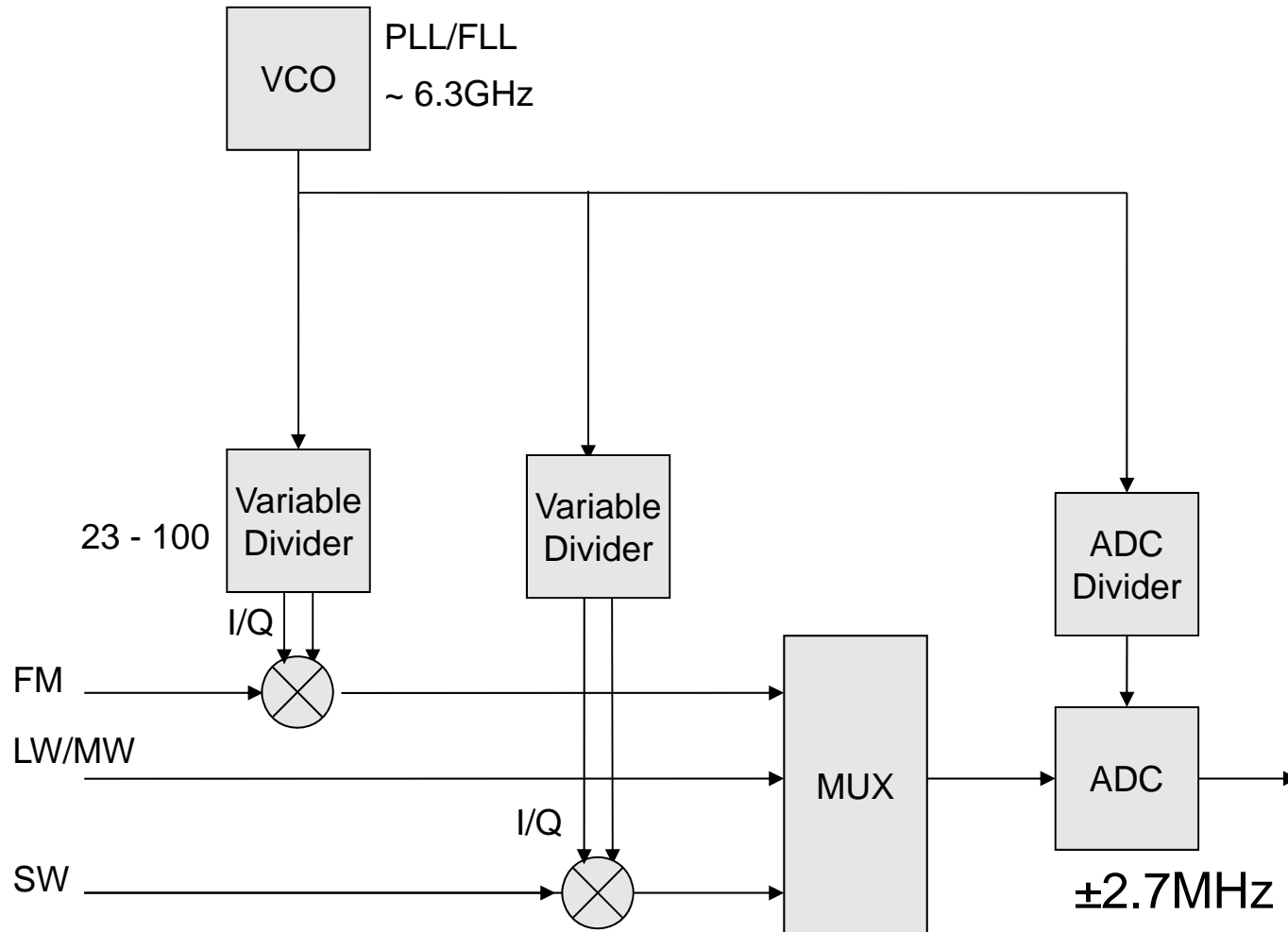
# Multi-Modulus Divider Outputs



# First Products with Fixed-Frequency Concept

- ▶ First products using the fixed-frequency oscillator concept were connectivity combo devices – FM/GNSS transceiver in 40nm TSMC
- ▶ First Car Radio product to use this concept is the NXP's TEF668x family, Single-Chip AM/FM Car Radio in 65nm TSMC
- ▶ System parameters:
  - ▶ PLL frequency = 6.3GHz, IF-ADC bandwidth =  $\pm 2.7$ MHz, divider range: 23-100
- ▶ Note: due to narrower ADC bandwidth, no fixed divider-by-2, requiring quadrature LO generation using odd divider ratios
  - ▶ Novel divider architecture, also providing programmable harmonic rejection
- ▶ Very successful product (best in class price/performance)
  - ▶ Japanese and Chinese Aftermarket
  - ▶ Also being designed in by number of USA/Europe OEMs

# LO Generation Using Fixed-Oscillator



# Future of Fixed-Frequency Concept



- ▶ Bluetooth and WiFi communication standards are essential for connectivity combos and IoT applications
- ▶ These applications would also benefit from the fixed-frequency concept
- ▶ Challenging requirements
  - High frequencies, wide channels, Frequency Hopping
- ▶ Innovation program addressing:
  - Wideband ADC, RF-DAC, HF divider architectures, PA linearization techniques, digital signal processing, 28nm process node
- ▶ Ultimate goal:
  - Disruptive approach to LO generation, using only one simple PLL for all connectivity standards