Technologies for integrated millimeter-wave antennas: An endless controversy?

Ulf Johannsen

October 9, 2012

CWT/e UHDR program (2008)

Vision 2017

Home, office, hospital

10Gbps wireless access point

100Gbps wireless backbone (RF or FS Optical)

Massive 2D/3D beamforming w/o FE

Fixed clients for data & streaming AV 10Gbps with QoS

Wall Via (RF or near-field E or M) Incl. 1-way wireless power

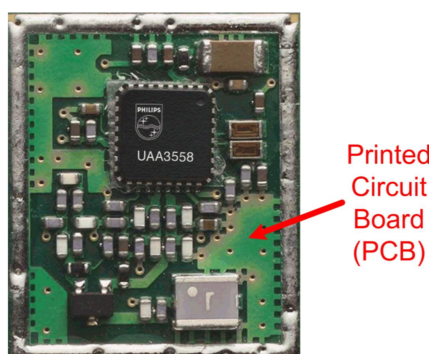
Antenna On Chip (AoC)?

Fiber

FTTH gateway to backbone

mobile & home portable client
Cognitive/SDR (BB+RF+FE)
4G mobile + 10Gbps in-home access
For fast content synchronization

What is an Antenna-on-Chip?



Printed Circuit Board (PCB)

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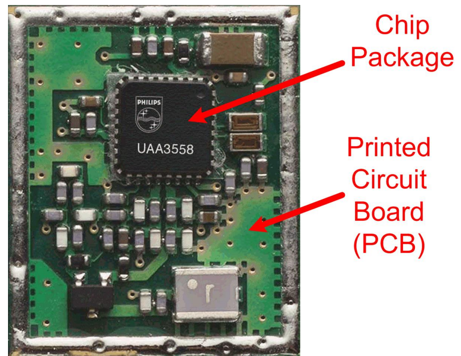

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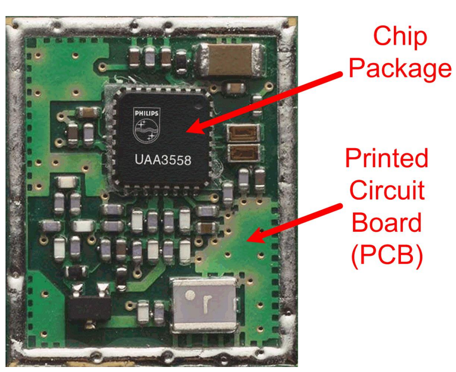

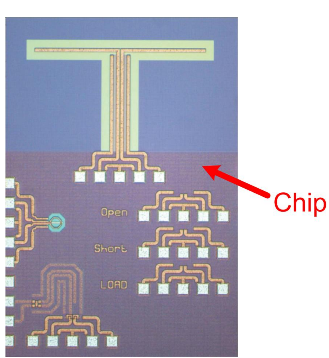

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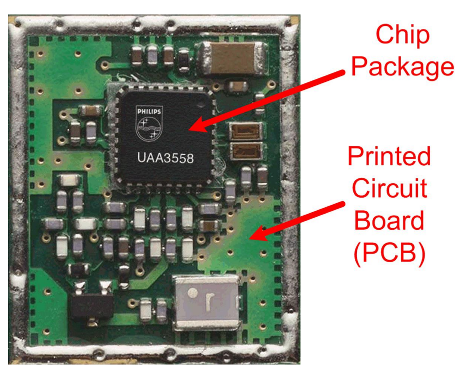
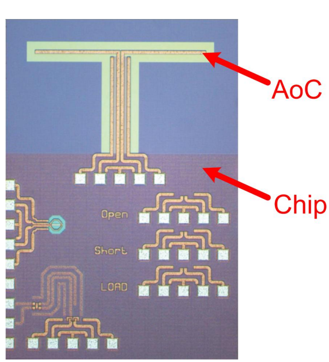
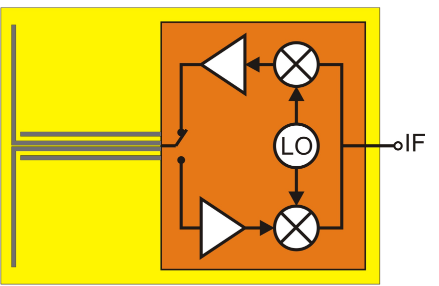




Why on-chip?



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- Direct matching of antenna and amplifier
- Antenna size at mm-waves makes it affordable

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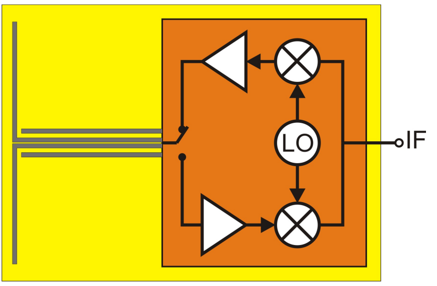

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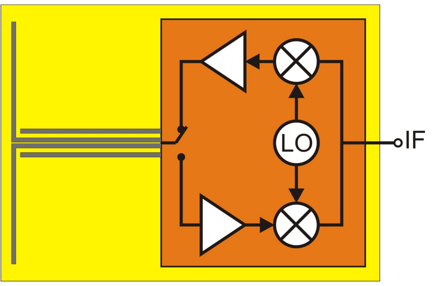

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The controversy

Well, that’s a good idea then!?

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- silicon is too lossy
- radiation efficiency is too low
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Who’s right?

Outline

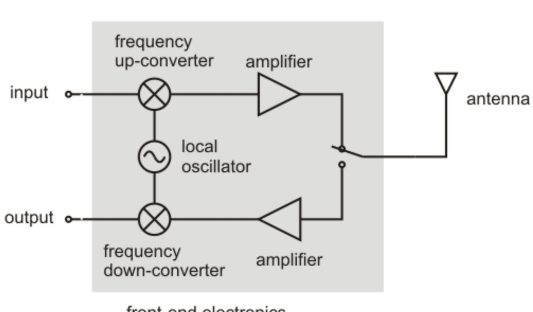
Antenna-in-Package

Antenna-on-Chip

Hybrid concept

Conclusions

Antenna-in-Package concept



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- high frequency in-/output reduced to IF

⇒ High performance and ease of use!

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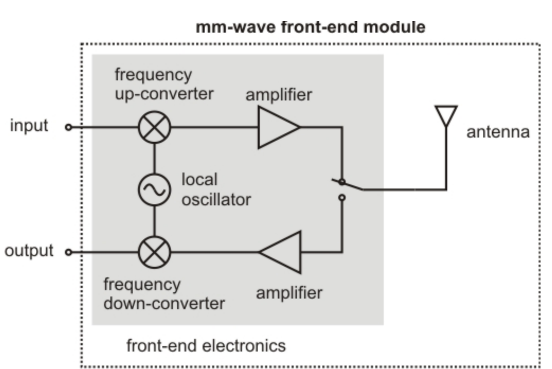

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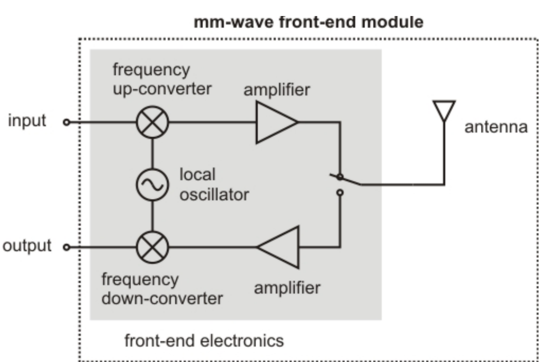

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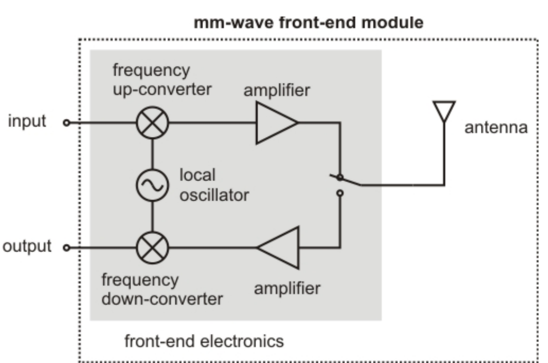

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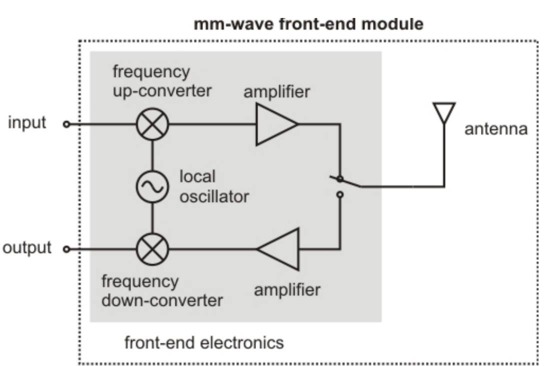

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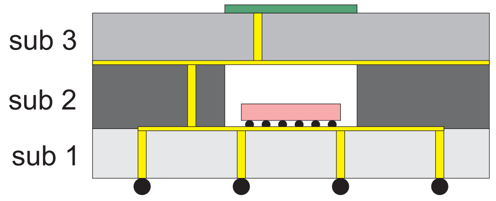
$\Rightarrow$ High performance and ease of use!

A typical solution

A generalized typical solution could look like this:



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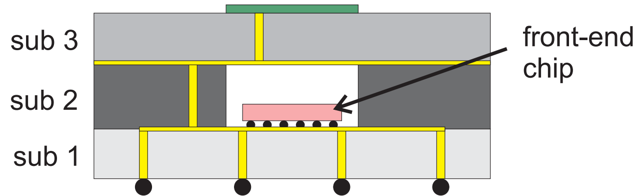

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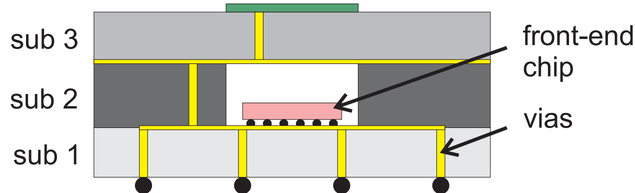

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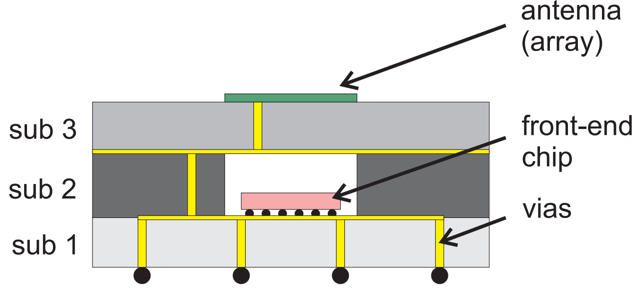

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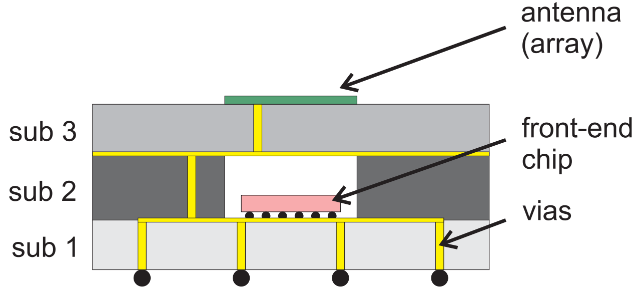

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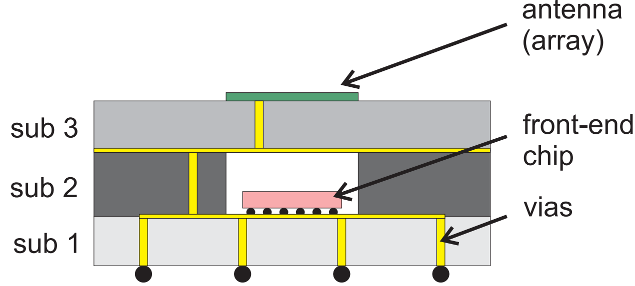

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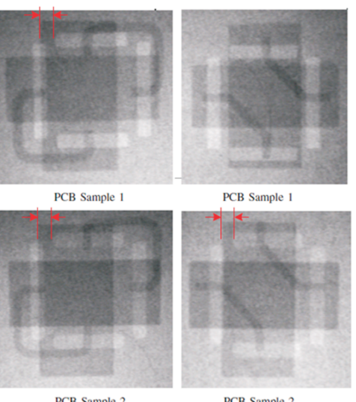
Stacked standard PCB technology

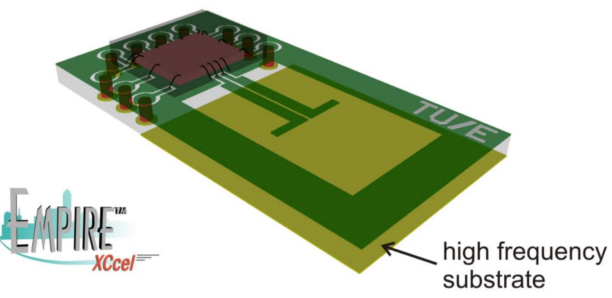
... the alignment in multilayer PCB technology poses a challenge[1]:



[1] M.I. Kazim, et al., "Half truncated icosahedral passive electromagnetic deflector for the 60 GHz band," EuCAP 2010, pp.1-5

Our proposal (1/2)

This is what we came up with instead:



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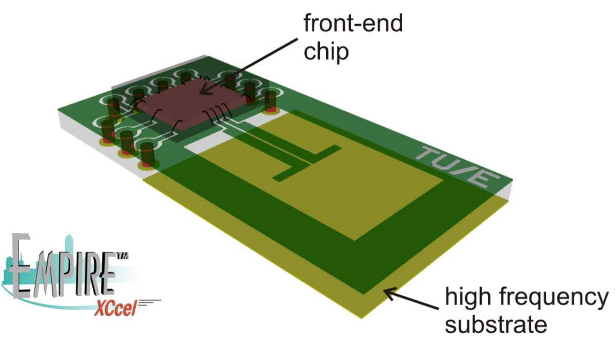

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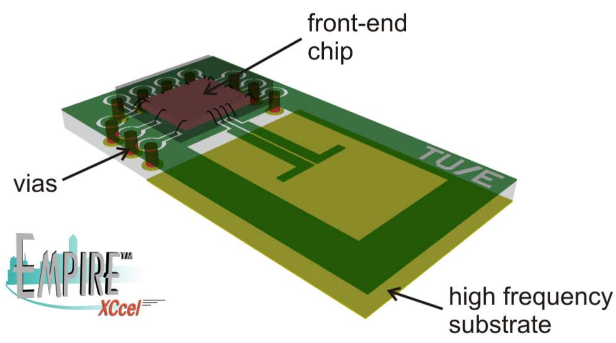

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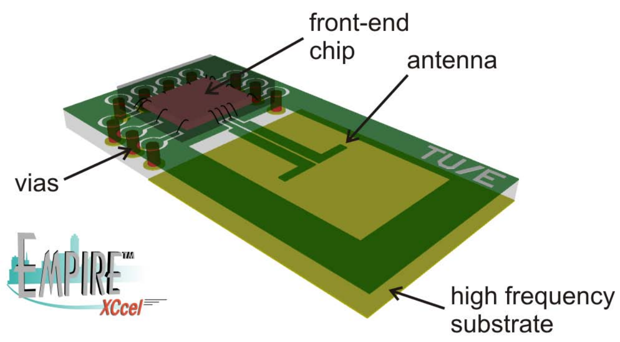
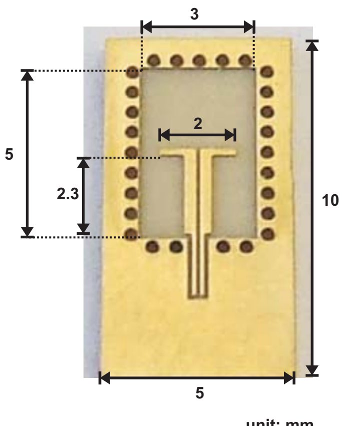


Design tape-out



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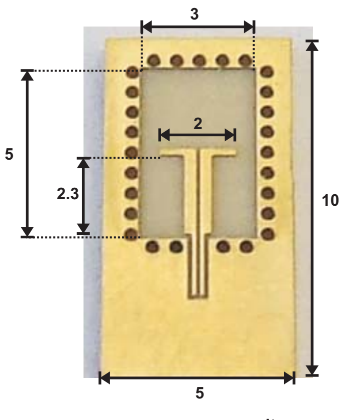
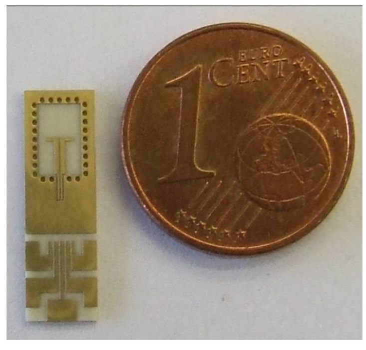
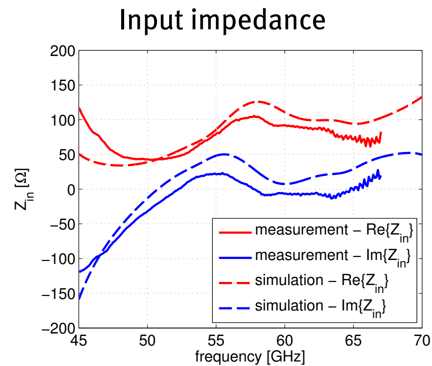


unit: mm



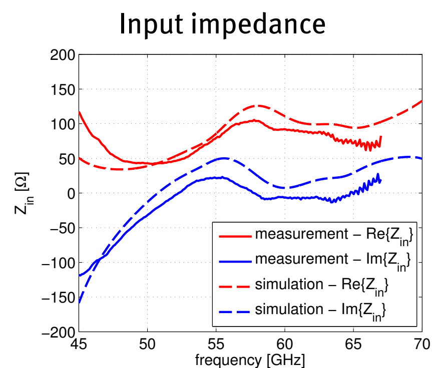
Measurement setup

Measurement results

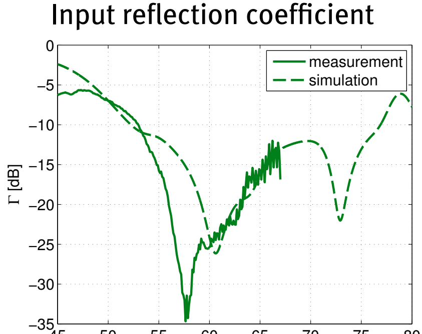


Measurement results

Input impedance

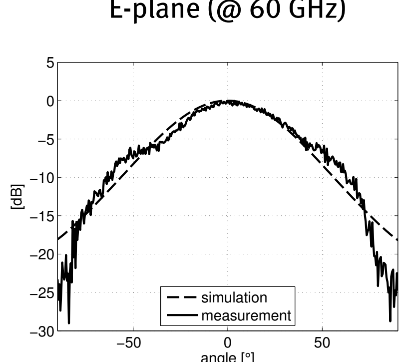


Input reflection coefficient

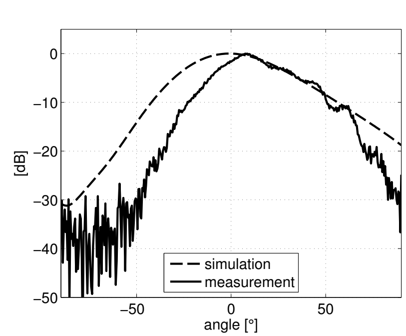


Measurement results

E-plane (@ 60 GHz)



H-plane (@ 60 GHz)



max. gain: ≈ 10 dBi

Radiation efficiency

$$\mu_{\mathrm{rad}} = 93\ \%$$

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$\mu_{rad} = 93\ \%$

including interconnect[2] with $S_{21} = -0.65$ dB:

[2] K. Pressel, et al., "Embedded wafer level ball grid array (eWLB) technology for system integration," CPMT Symposium Japan, 2010

Radiation efficiency

$\mu_{rad} = 93\ \%$

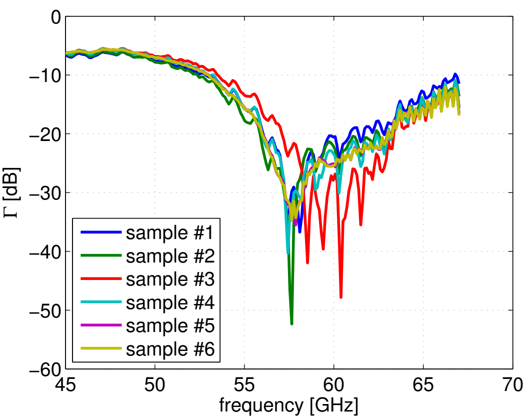
including interconnect[2] with $S_{21} = -0.65$ dB:

$\mu_{rad} = 80\ \%$

[2] K. Pressel, et al., "Embedded wafer level ball grid array (eWLB) technology for system integration," CPMT Symposium Japan, 2010

Yield analysis

A quick yield analysis:



Antenna-in-Package

Antenna-on-Chip

Hybrid concept

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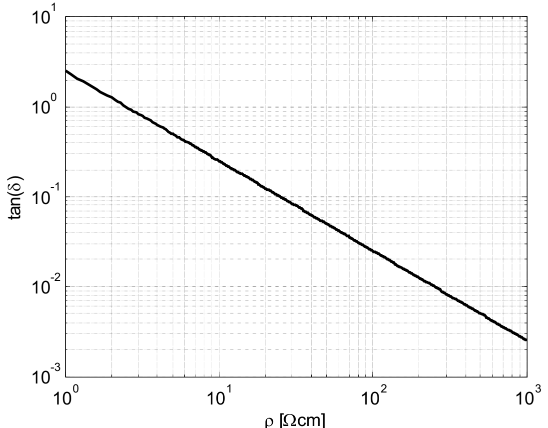
Silicon losses

Resistivity in microwave terms



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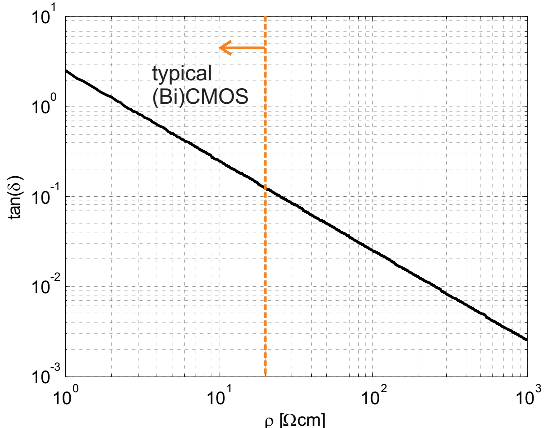

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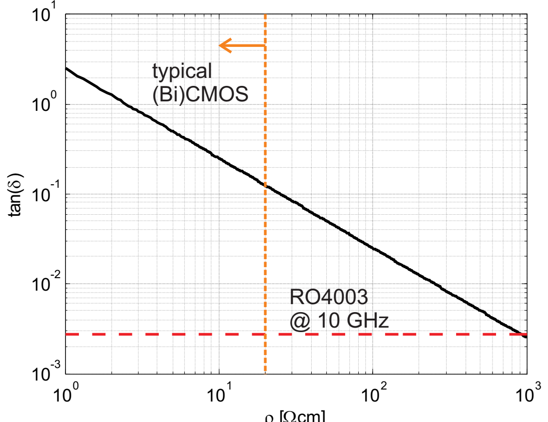


Test-chip

2

metal plate

LOAD Short Open

1.5

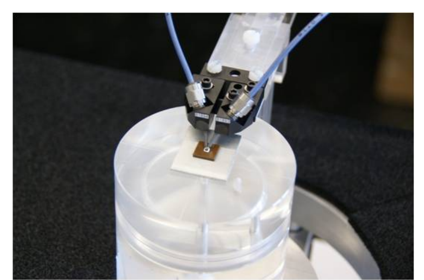
1.086

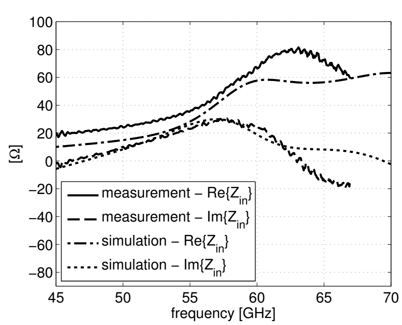
0.63

0.05

unit: mm

silicon ground down to 200 μm




100
80
60
40
20
0
−20
−40
−60
−80
[Ω]
45
50
55
60
65
70
frequency [GHz]
measurement – Re{Z_in}
measurement – Im{Z_in}
simulation – Re{Z_in}
simulation – Im{Z_in}

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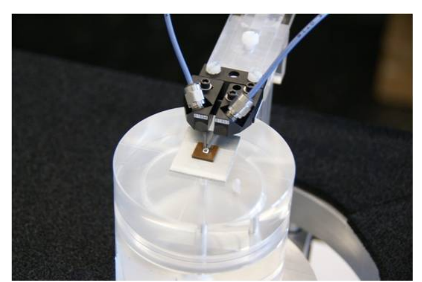
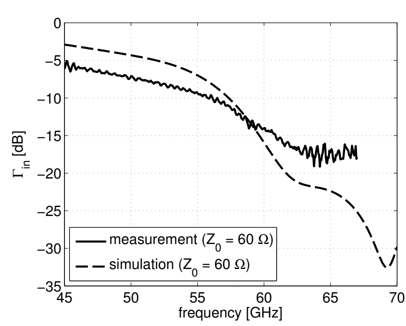
Measurement results - on-chip probing





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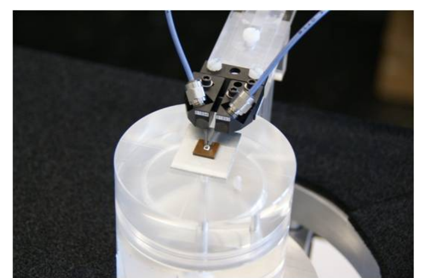

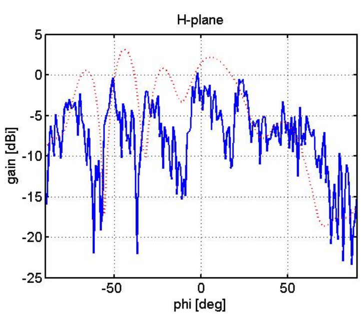

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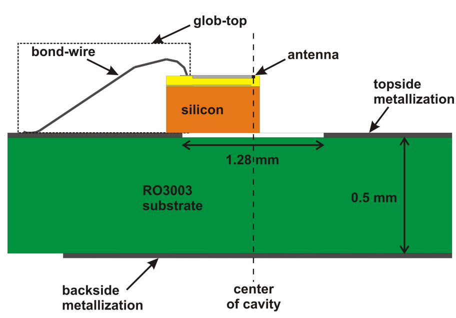

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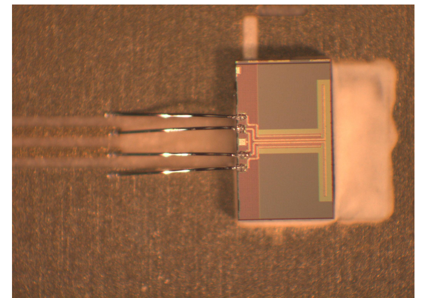

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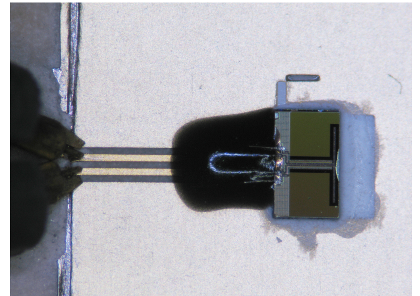

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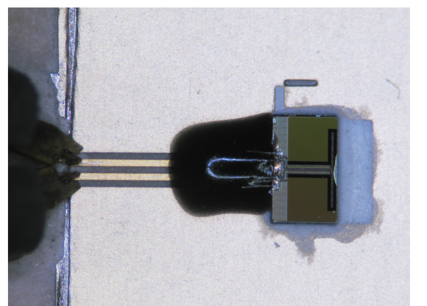

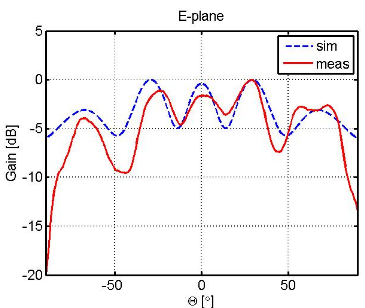

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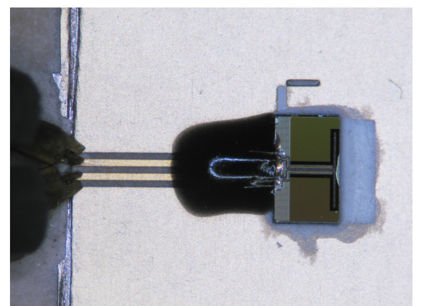

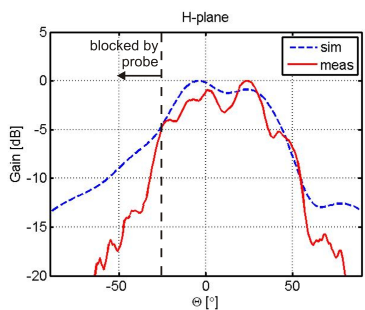

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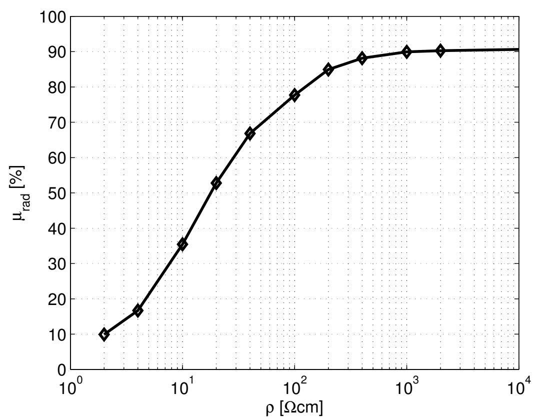

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Radiation efficiency

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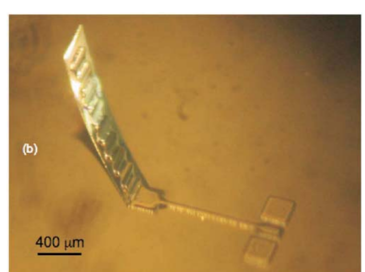

[3] A. Mahanfar, et al., IEEE Trans. A&P, vol.58, no.9, pp.3020-3028, Sept. 2010

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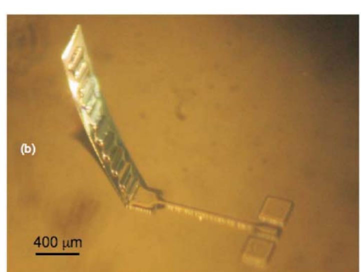

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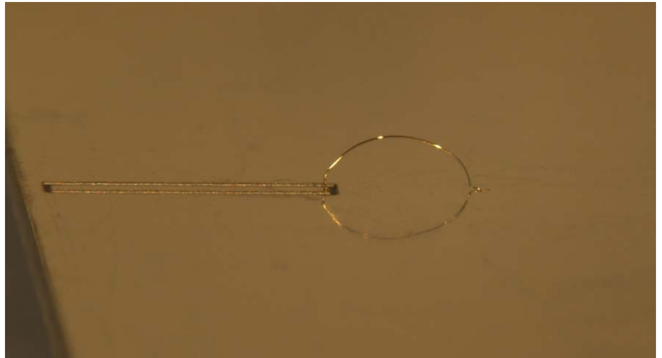
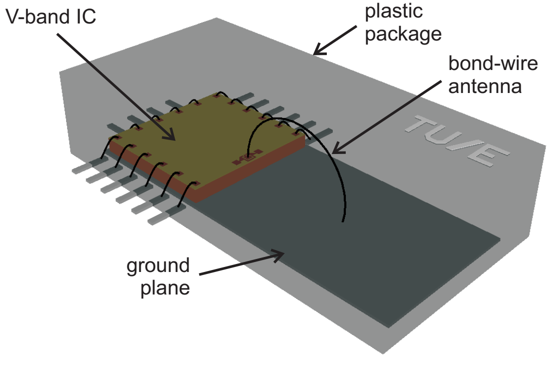


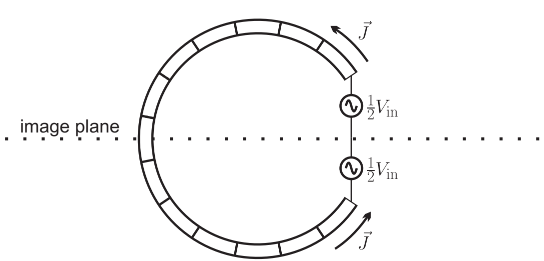
wire-bond technology!

Hybrid concept

Use a standard, low-cost technology, e.g.,



wire-bond technology!

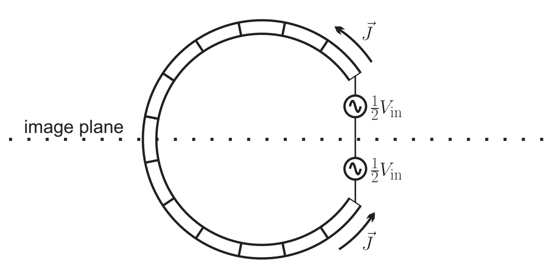


Integral equation:

$$\left\{\vec{E}_{\text{gen.}}(\varphi)\right\}_{\varphi} = \frac{j\eta}{4\pi}\int_{\varphi'}\left[kb\cos(\varphi-\varphi') + \frac{1}{kb}\frac{\partial^2}{\partial\varphi^2}\right]\frac{e^{-jkbR_b(\varphi-\varphi')}}{R_b(\varphi-\varphi')}I(\varphi')d\varphi', \tag{1}$$

with

$$R(\vec{r}-\vec{r}') = R(\varphi-\varphi') = \sqrt{4\sin^2\left(\frac{\varphi-\varphi'}{2}\right)+\left(\frac{a}{b}\right)^2}. \tag{2}$$



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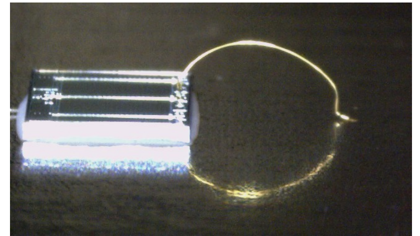
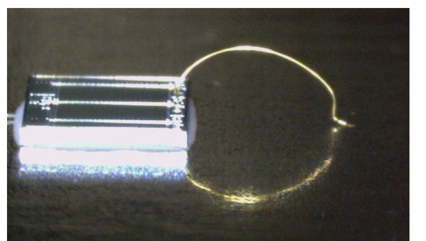
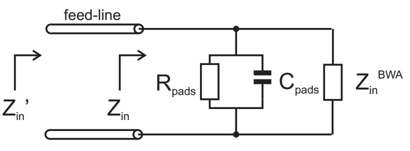
TU/e Technische Universiteit Eindhoven University of Technology

Prototype



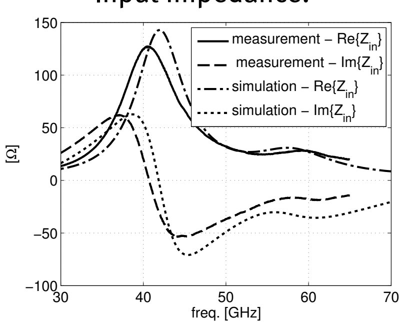
Prototype





Measurements

Input impedance:



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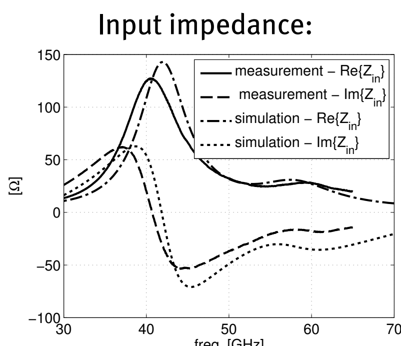


Radiation efficiency:

μ_{rad} [%]

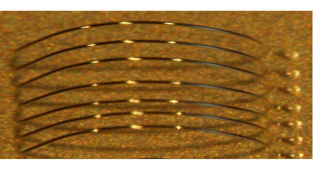
freq. [GHz]

$$\mu_{\text{rad}} = \frac{\text{Re}\left\{Y_{\text{in}}^{\text{BWA}}\right\}}{Y_{\text{pads}} + \text{Re}\left\{Y_{\text{in}}^{\text{BWA}}\right\}}$$

Yield analysis (1/2)

What about yield?

Yield analysis (1/2)



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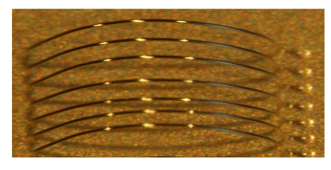

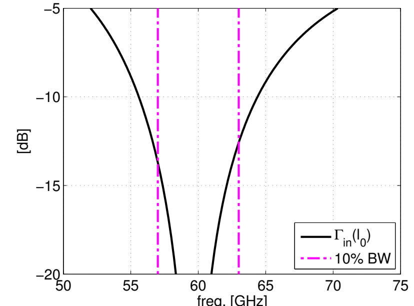

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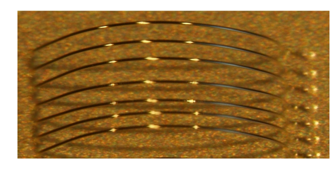

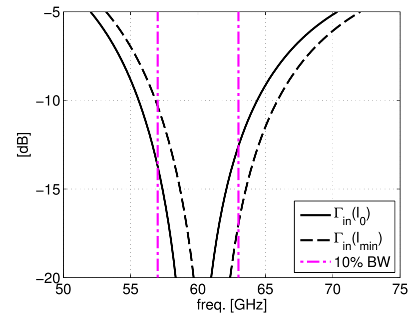

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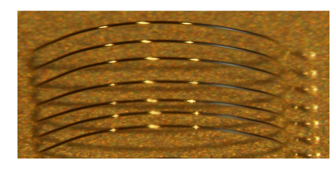

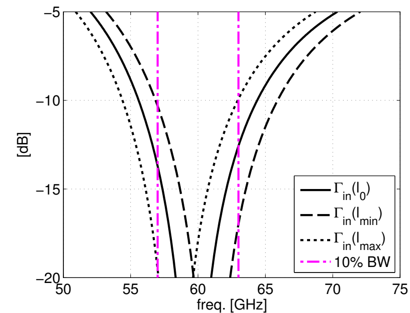

Yield analysis (1/2)

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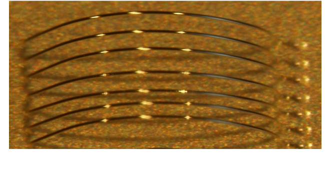

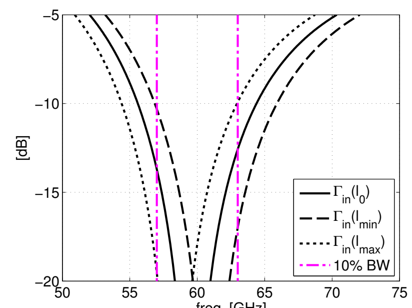

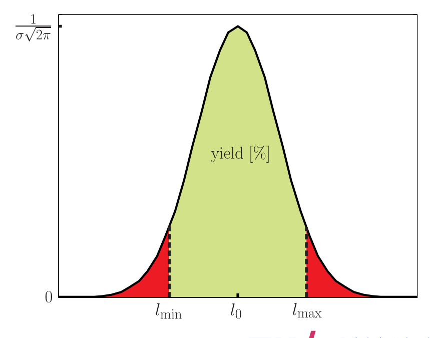

Yield analysis (2/2)

f_0 [GHz]	l_0 [mm]	l_{min} [mm]	l_{max} [mm]	yield [%] ($3\sigma_1 = 25\ \mu$m)	yield [%] ($3\sigma_2 = 50\ \mu$m)
30	5.498	5.438	5.557	100	99.97
60	2.733	2.668	2.793	100	99.97
100	1.665	1.605	1.725	100	99.97
150	1.131	1.086	1.186	100	99.61
200	0.864	0.824	0.909	100	98.83
250	0.707	0.677	0.740	99.98	94.02
270	0.654	0.634	0.681	99.12	83.23
300	0.594	0.587	0.609	76.36	47.87

Conclusions

What's the best technology then?

	design flexibility	direct matching	μ_{rad}
AiP	high	no	80 %
AoC	moderate	yes	45^{+} %
Hybrid	low	yes	80 %

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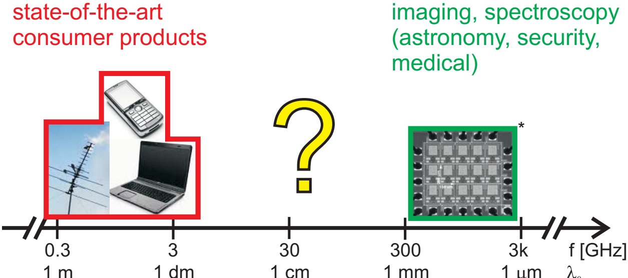

* E. Ojefors, U.R. Pfeiffer, A. Lisauskas, H.G. Roskos, "A 0.65 THz Focal-Plane Array in a Quarter-Micron CMOS Process Technology," Solid-State Circuits, IEEE Journal of , vol.44, no.7, pp.1968-1976, July 2009

An endless controversy?

Probably yes!

An endless controversy?

Probably yes!

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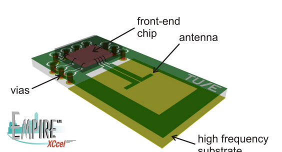
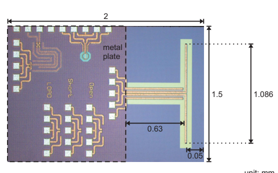
That’s it, folks...





Thank you!