Towards Low Low Power

Designing with Energy Awareness in Mind….

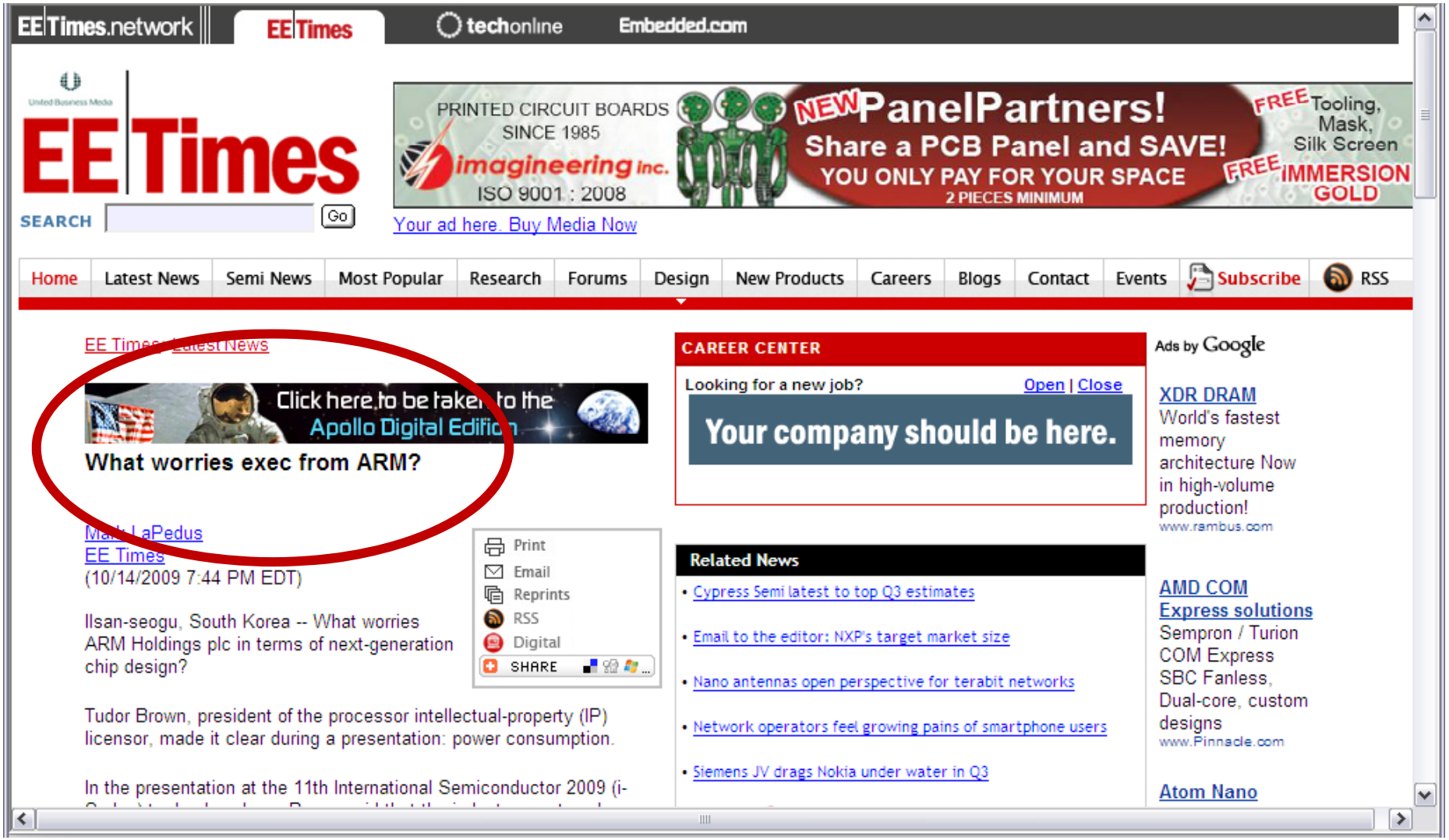
José Pineda de Gyvez

jose.pineda.de.gyvez@nxp.com

NXP Semiconductors

Eindhoven University of Technology

What Worries Exec from ARM?



Ilsan-seogu, South Korea -- What worries ARM Holdings plc in terms of next-generation chip design?

Tudor Brown, president of the processor intellectual-property (IP) licensor, made it clear during a presentation: power consumption. In the presentation at the 11th International Semiconductor 2009 (i-Sedex) trade show here, **Brown said that the industry must work on lowering power consumption by 50 percent every two nodes. If it fails to address those issues, ''the industry could stall,'' he warned.**

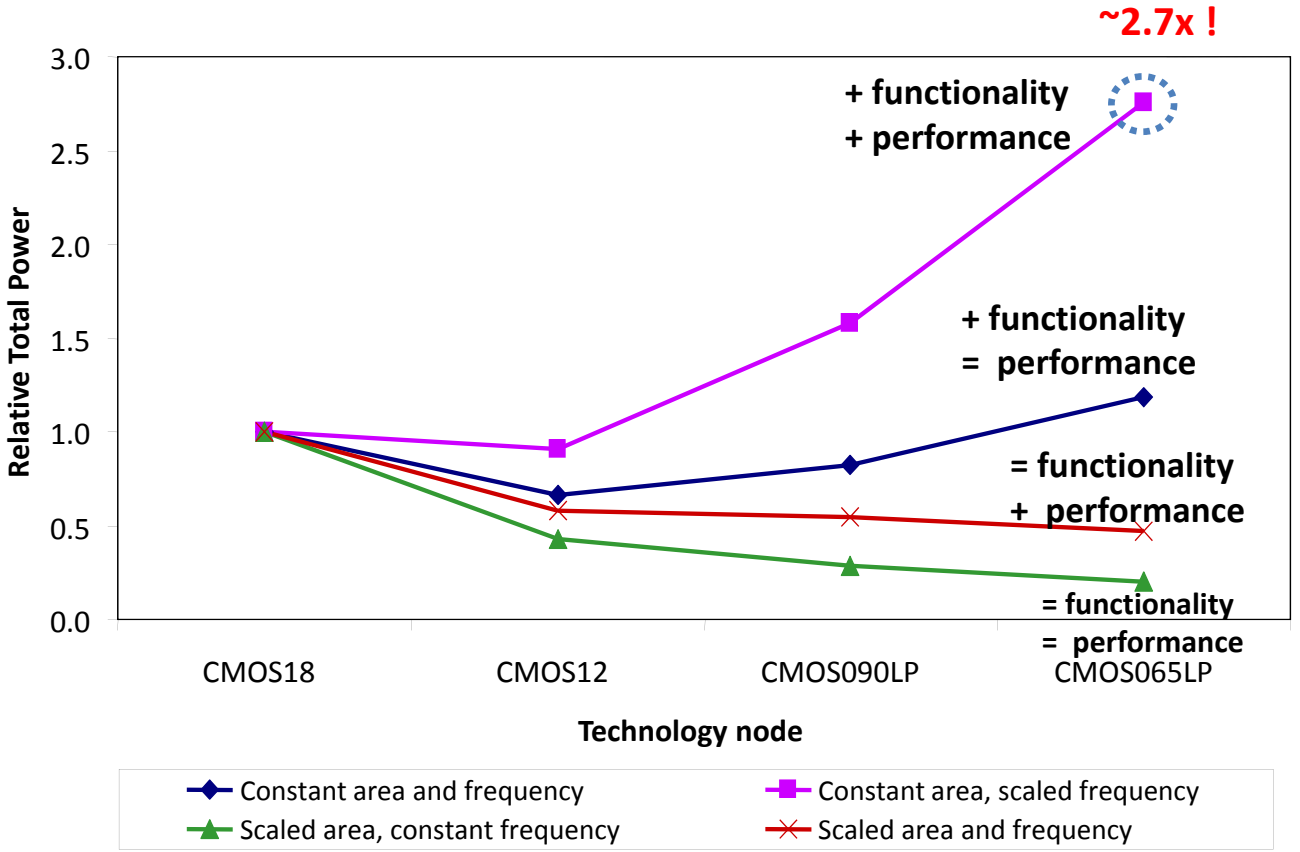
To address those concerns, he said designers must consider some of the following steps: **take a systems-level approach to the problem; use application-specific accelerators; address power in embedded memory designs; and look at multi-core processors**

Why do we need Power Management?

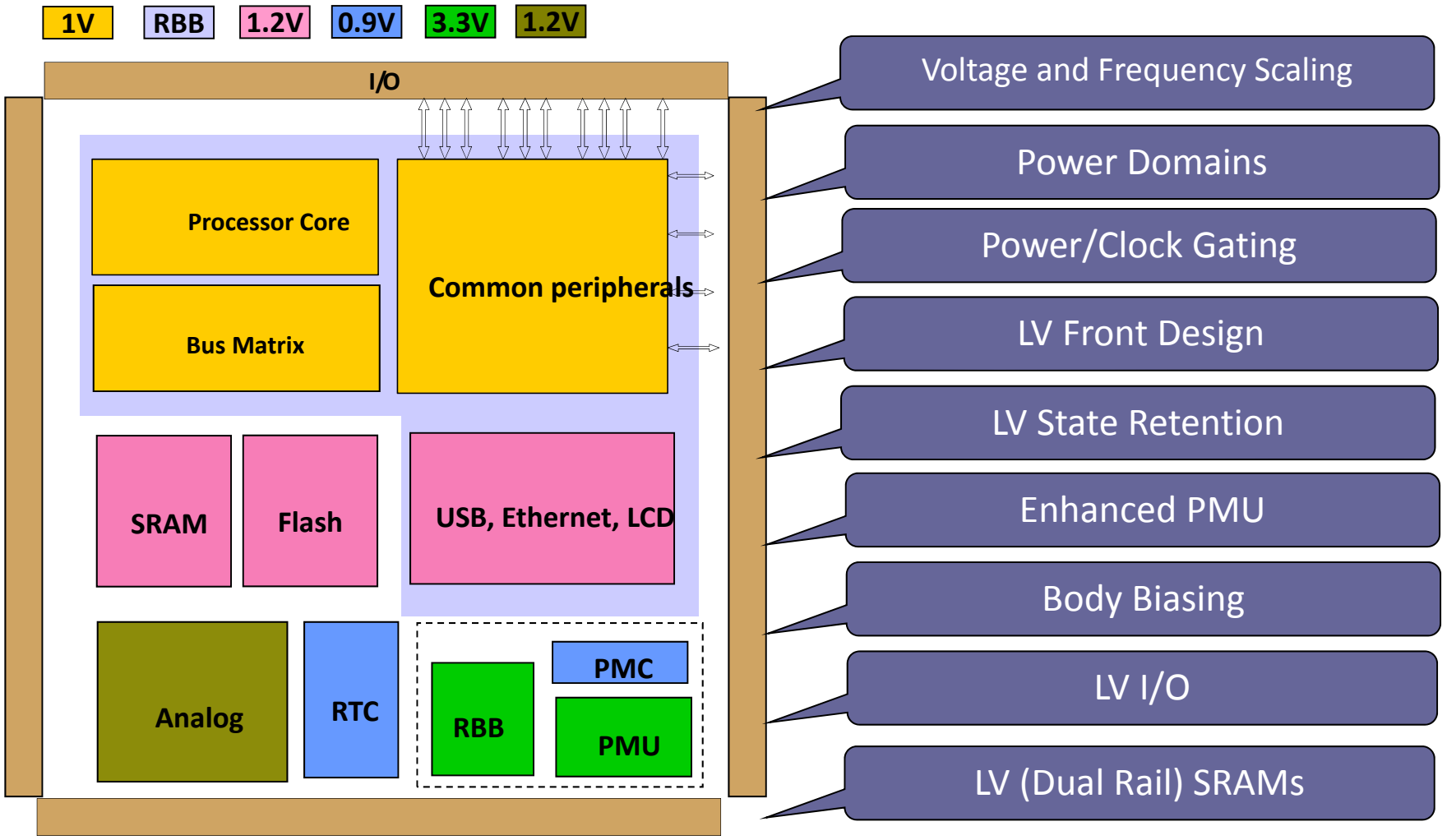
Ref. std-cell block in CMOS18:

- 50K flip-flops+1250K logic gates
- Logic depth of 25
- 100MHz operating frequency
- Area of library reference gate used for scaling reference.

- Scaling dependencies:
  - block area ~ s^2
  - operating frequency ~ 1/s
  - V_{dd} CMOS18 = 1.8V
  - V_{dd} others = 1.2V



Low Power Techniques

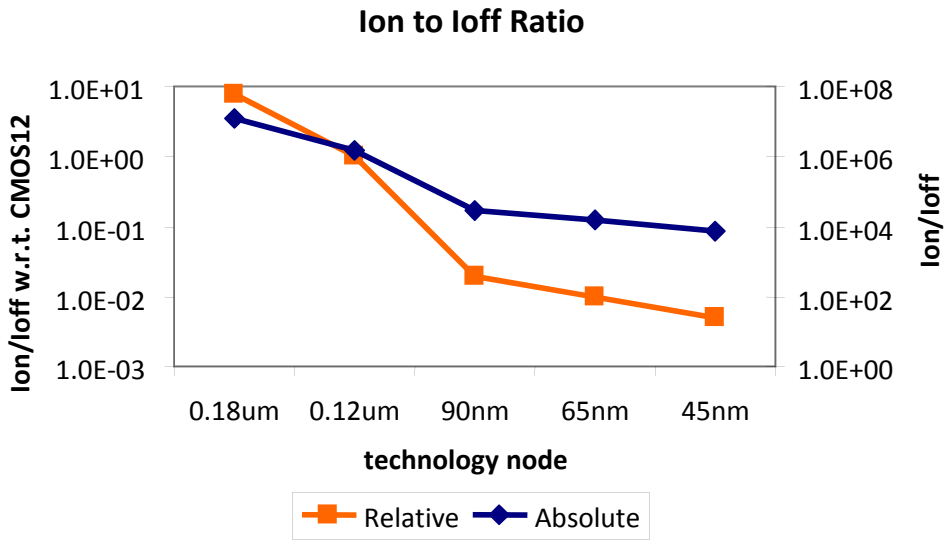


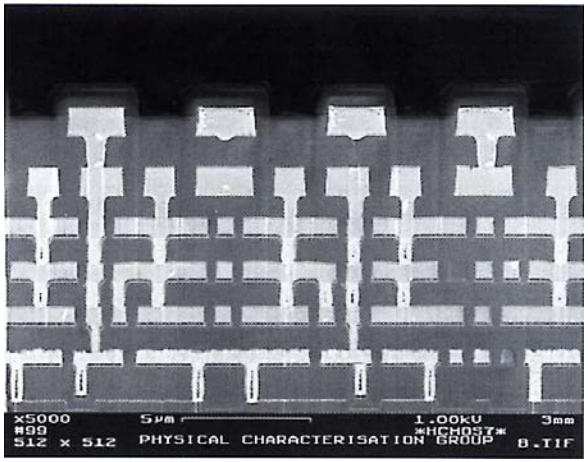
Outline

- Technology Outlook
- Dynamic Supply Voltage Scaling
- Minimum Supply Operation
- LV Designs

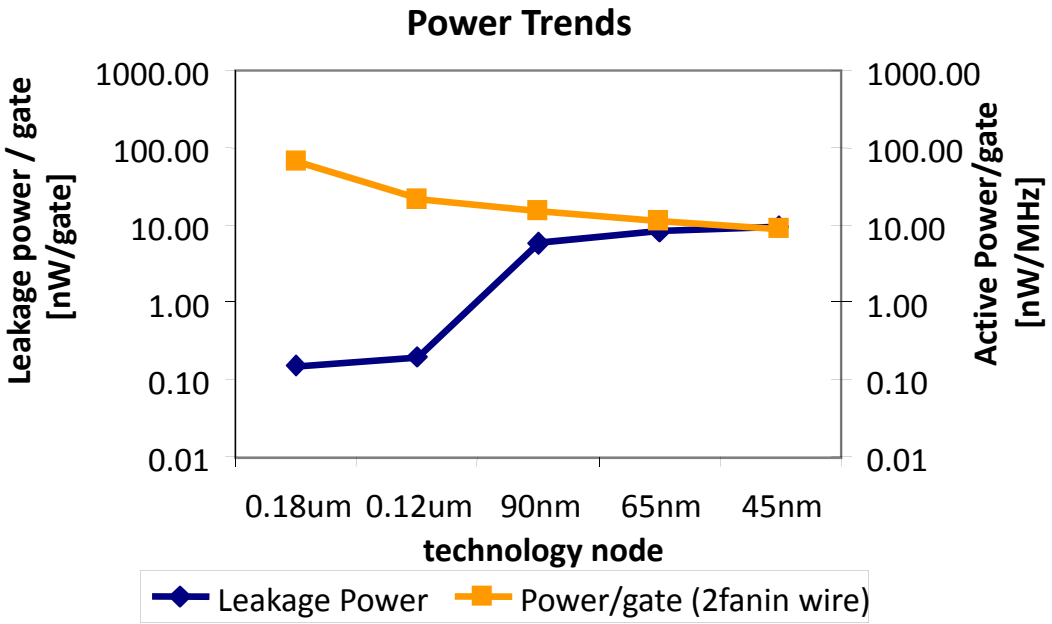
Technology Outlook

Technology Outlook





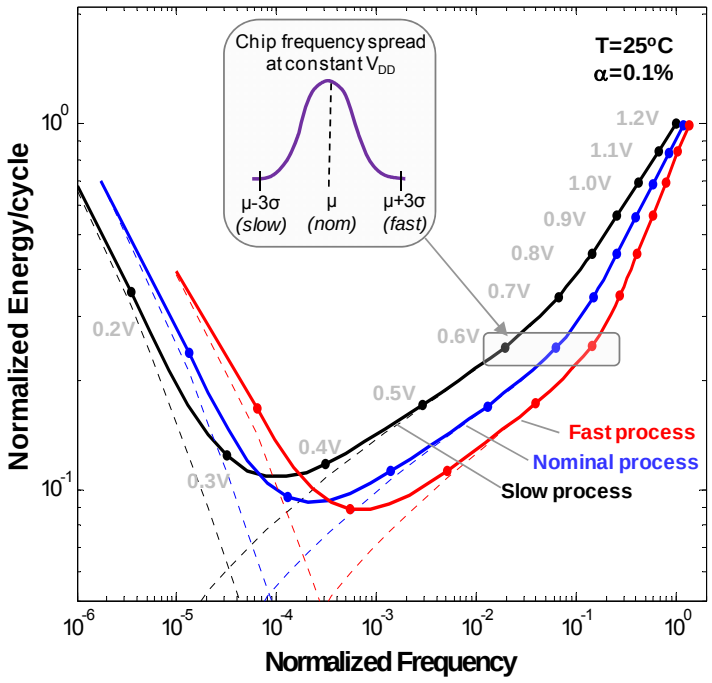
IC Density
(smaller transistors)

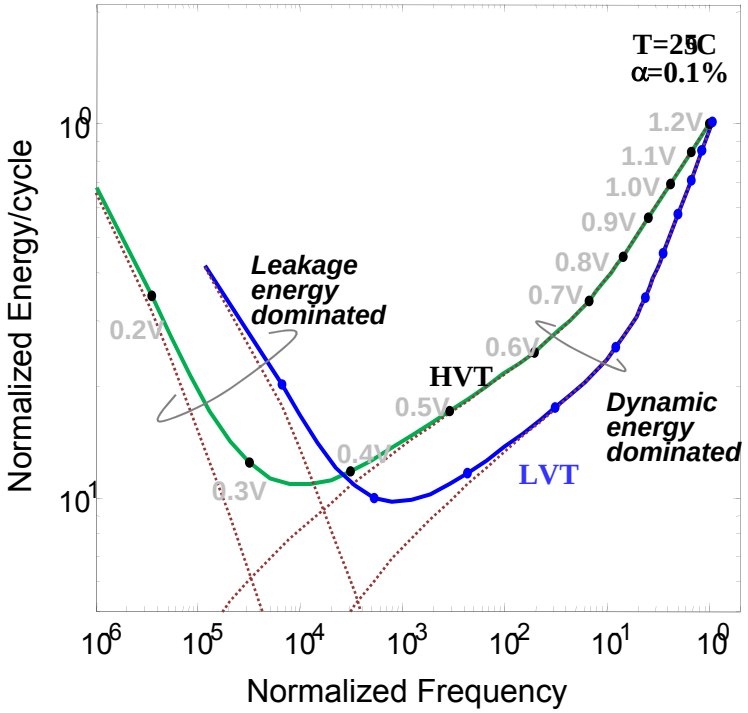


IC Functionality
(more transistors)

IC Performance
(faster/leaky transistors)

Impact of Technology on Minimum Energy Point

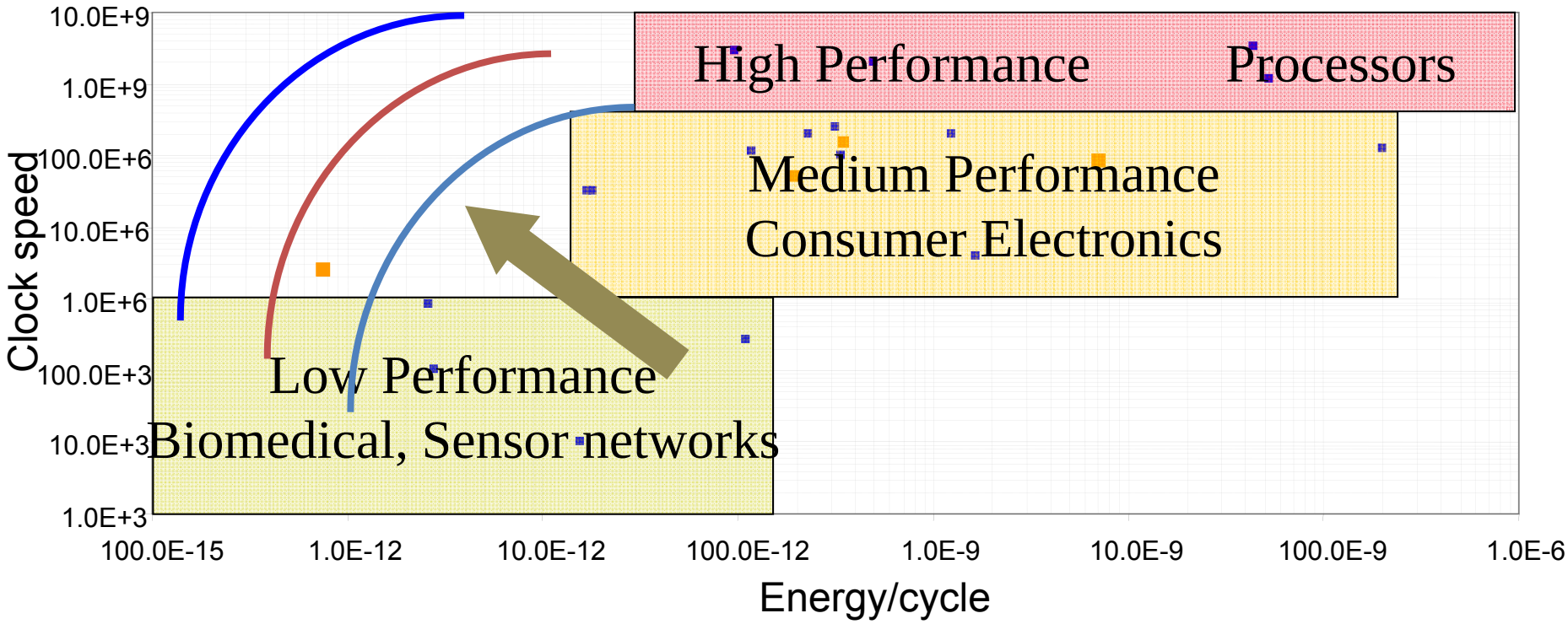




- Optimum energy point at very low supply voltages
  - ~10x lower energy
- Technology Dependence (HVT, LVT. corners)
  - Small performance difference at nominal VDD
  - ~10x performance difference below VDD/2

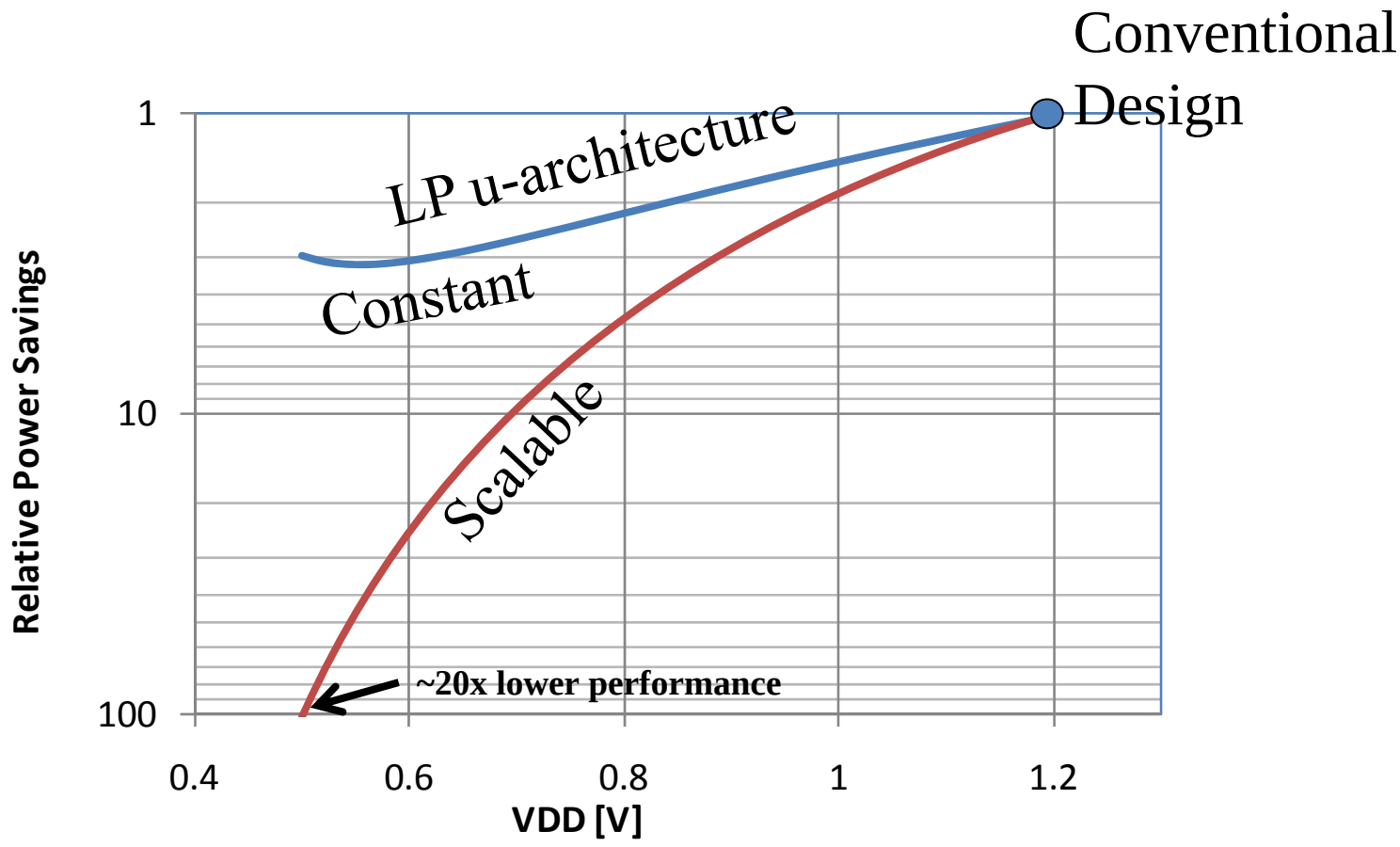
Dynamic Voltage Scaling

Low Power Landscape

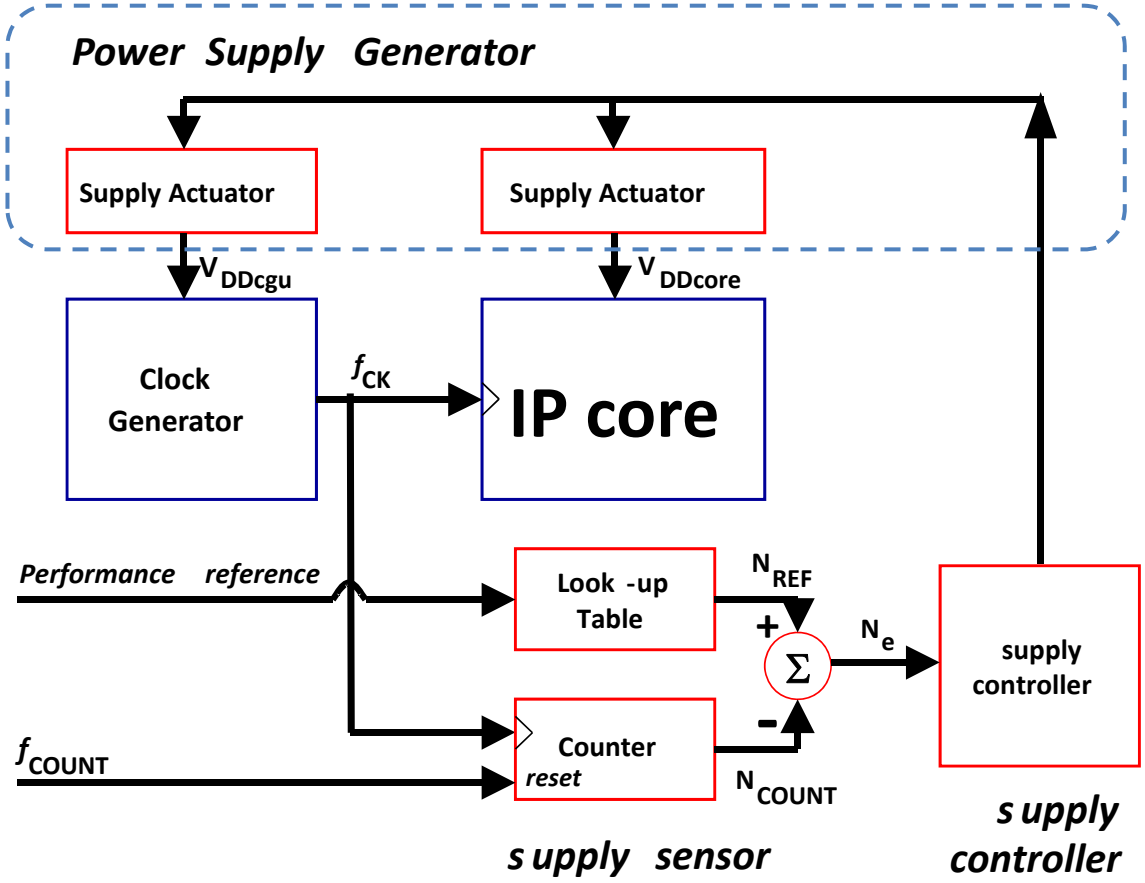


Dynamic Power Scaling Strategy

Constant vs. Scalable Throughput



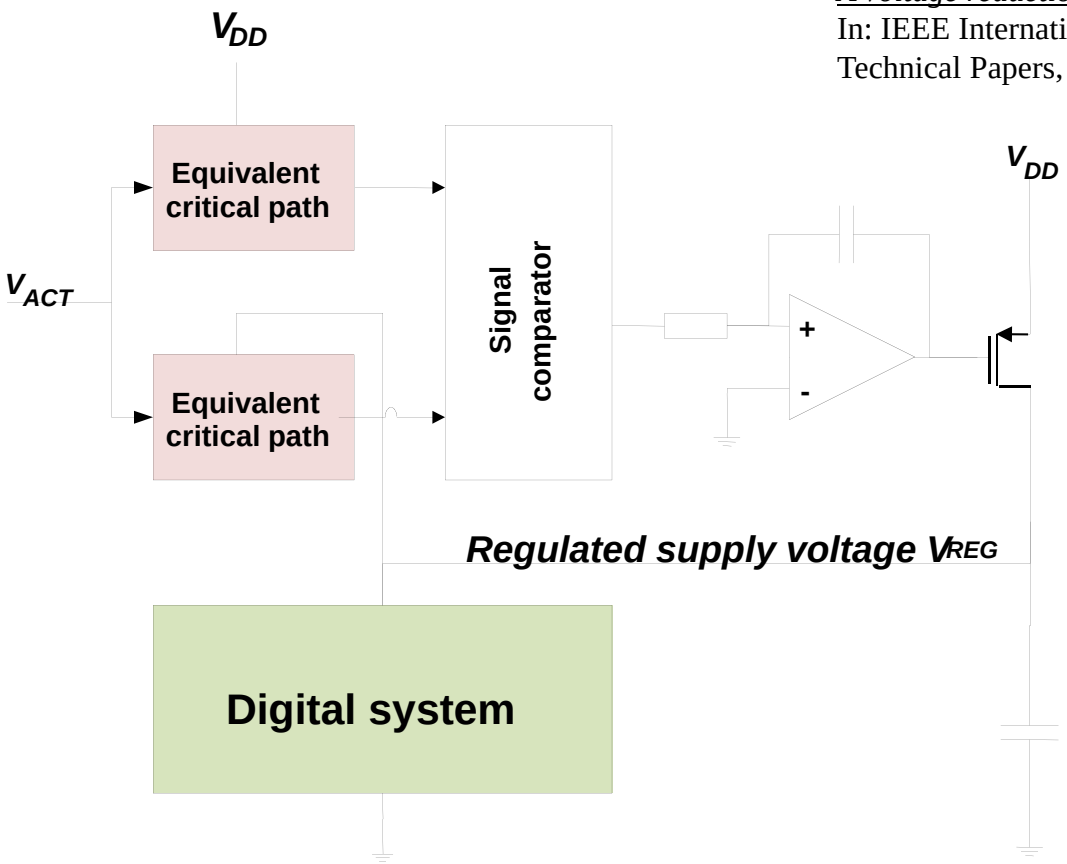
Power Supply Control



- Adjusts VDD against *design time* value
  - Cold-start offsets, process variations, operational drifts.
- Average-V_{DD} control.

Automatic VDD Control (1990)

Macken, P., M. Degrauwe, M. van Paemel and H. Oguey
A voltage reduction technique for digital systems.
In: IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, CA, USA, 16 Feb. 1990, p. 238-239



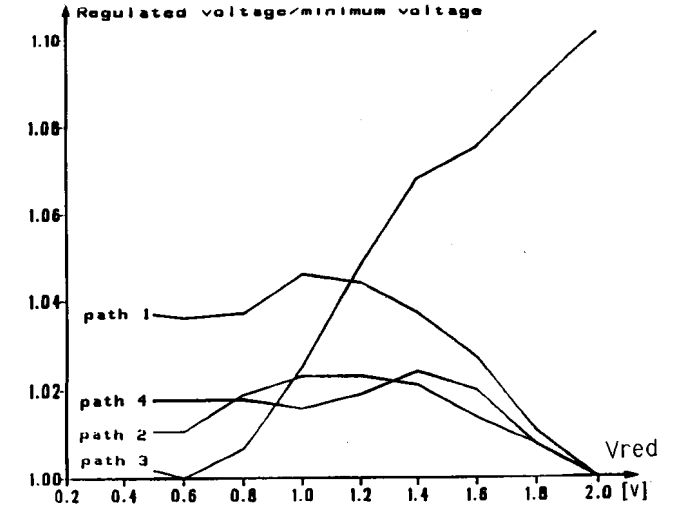
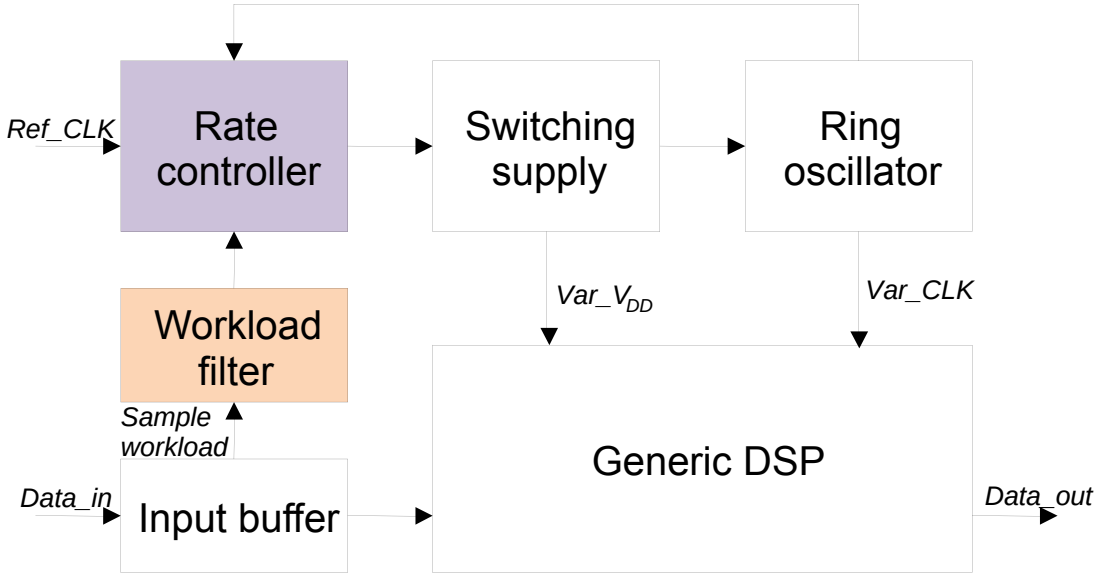


Fig. 8. Ratio of regulated voltage to the minimum voltage necessary to fulfill speed requirements.

- Ring oscillator to emulate critical path
- PLL based signal processing

Workload-based VDD Control

Gutnik, V. and A. Chandrakasan
Embedded power supply for low-power DSP.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Dec. 1997, Vol.5, No.4, p.425-435



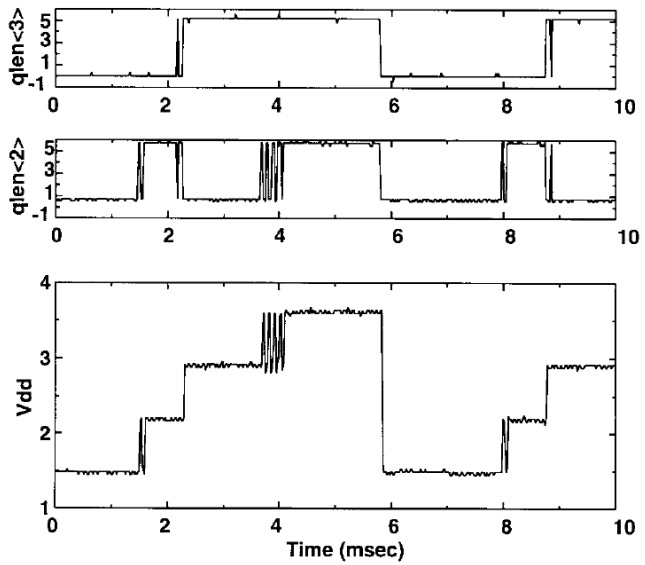
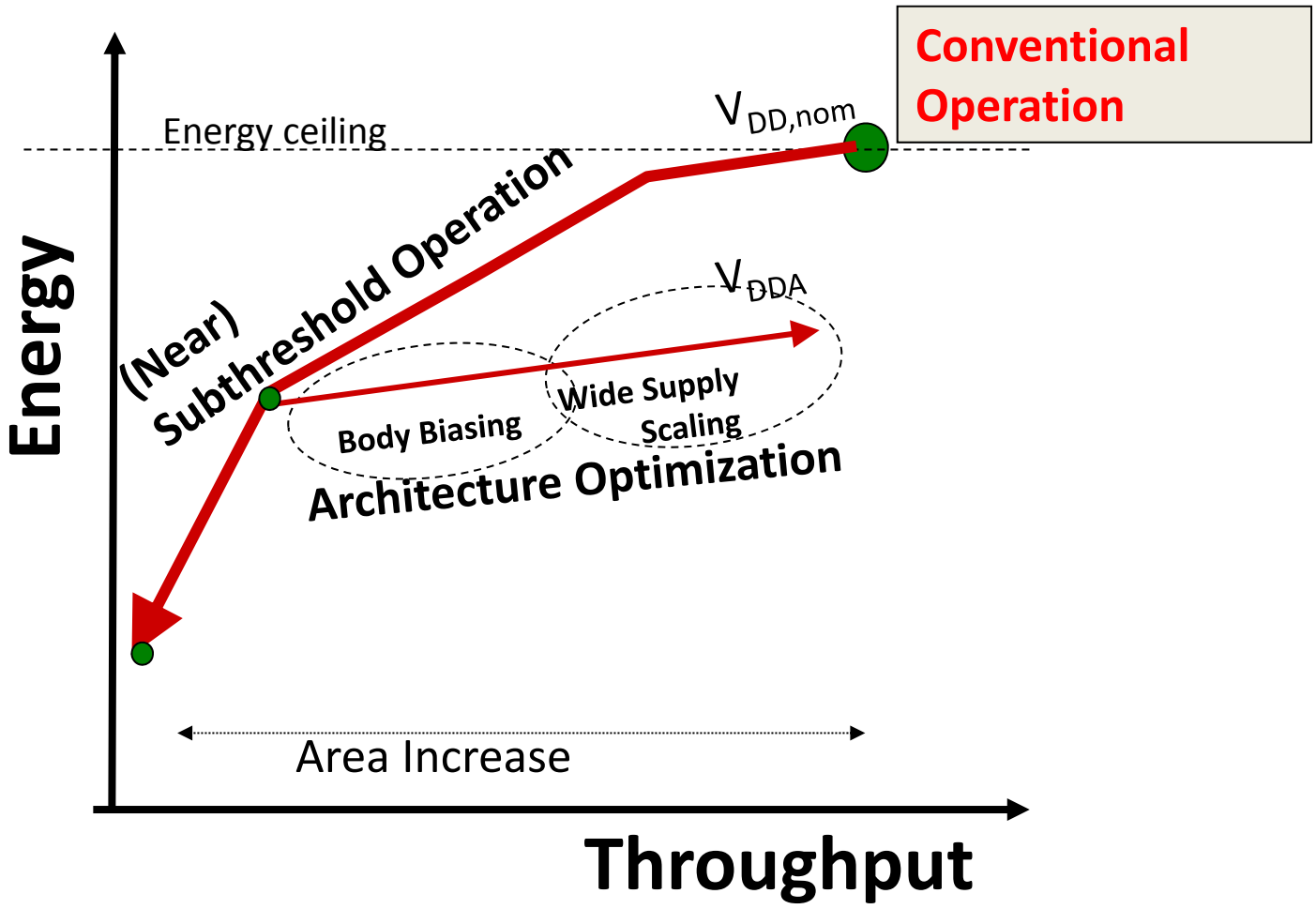


Fig. 19. Measured voltage levels.

- Workload filter is based on FIFO buffer queue
- Control loop controls queue over- and underflow
- System uses voltage dithering
  - LUT with major frequency steps
  - Dithering: mix of fast and slow processing due to voltage adjustment

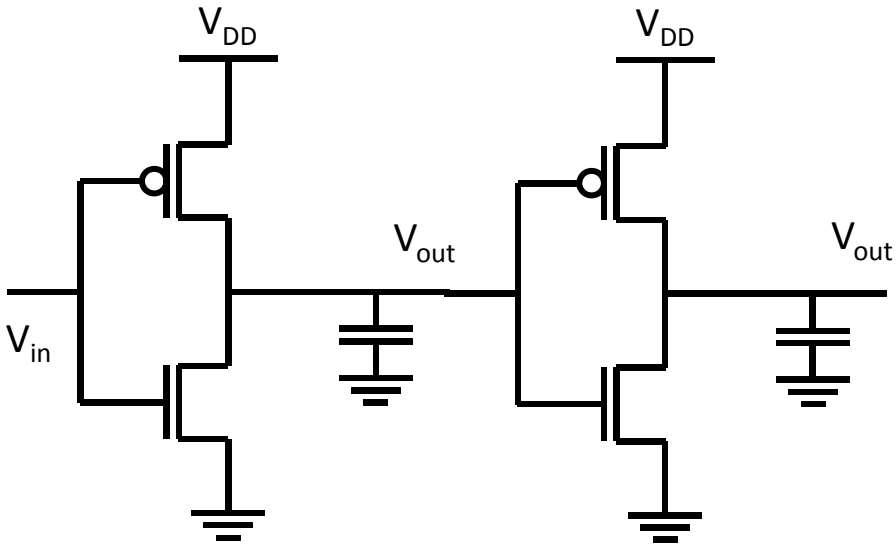
Minimum Supply Operation

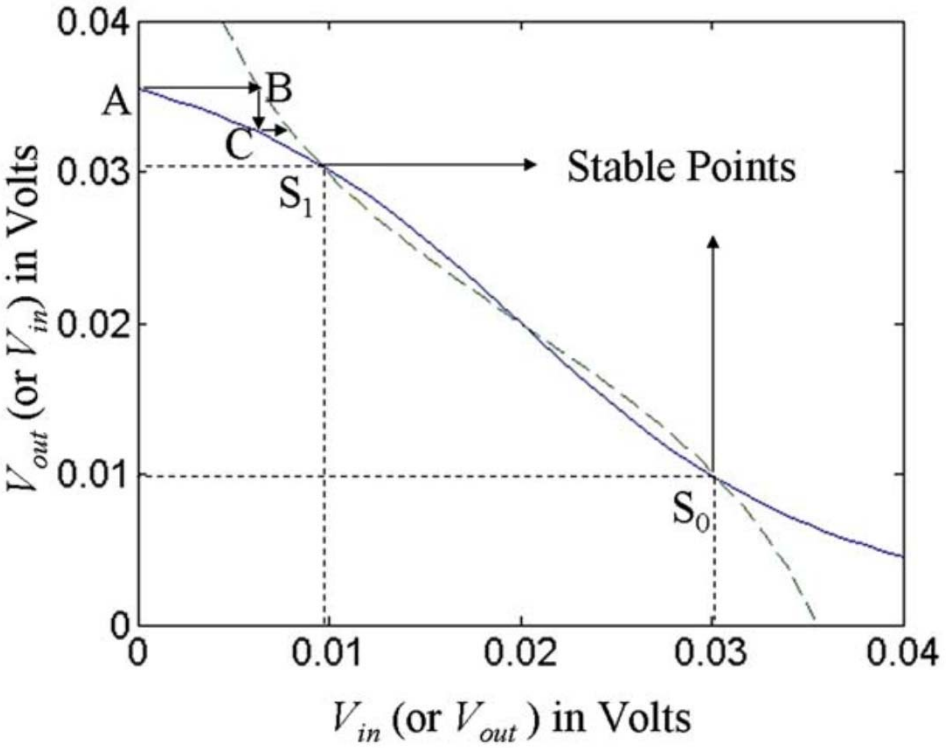
Low Voltage Design Challenges



Minimum Power Supply Voltage

We want to investigate the voltage swing of the inverter in subthreshold

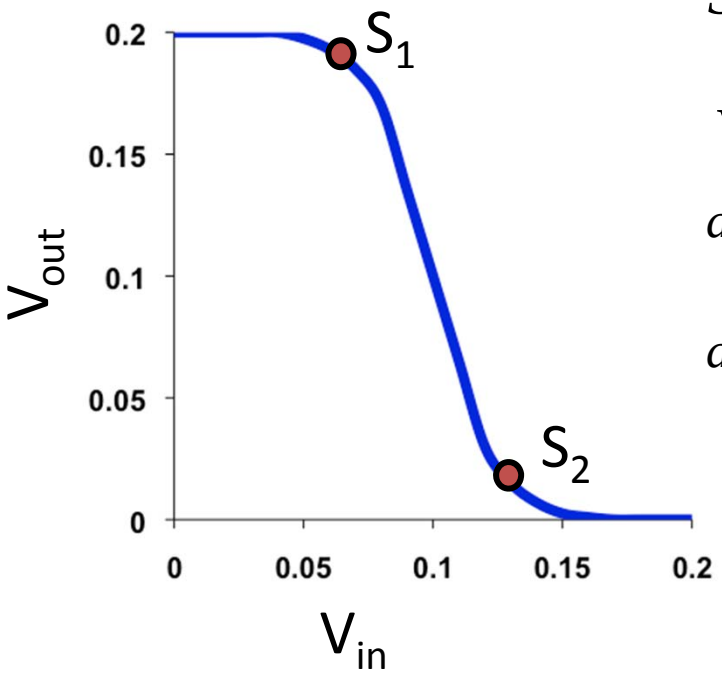




S_1 and S_2 are two stable points

Compact models considering incomplete voltage swing in complementary metal oxide semiconductor circuits at ultralow voltages: A circuit perspective on limits of switching energy
Sumeet Kumar Gupta, Arijit Raychowdhury, and Kaushik Roy
JOURNAL OF APPLIED PHYSICS 105, 094901 2009

The steady state values of the output voltage corresponding to logic '1' and '0'



$$S_1 = (V_o, V_1) = \left(nU \ln a_o, nU \ln a_1\right)$$

$$S_2 = (V_1, V_o) = \left(nU \ln a_1, nU \ln a_o\right)$$

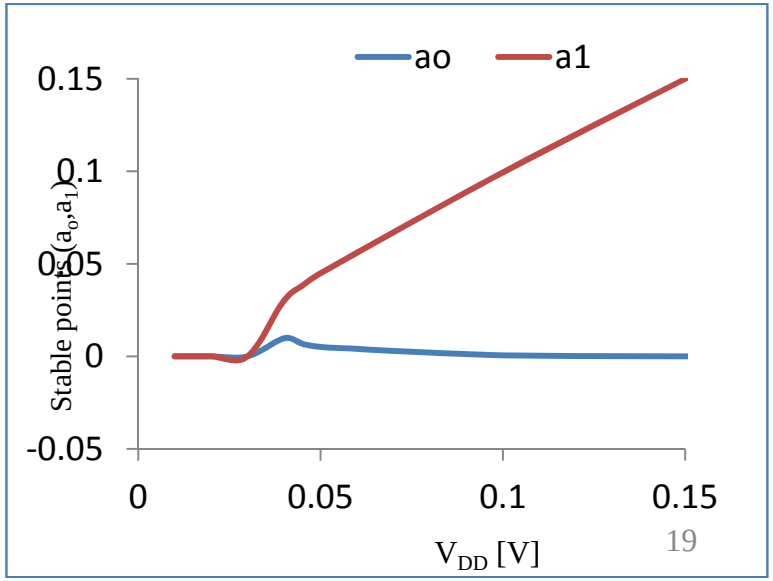
Note that $V_o + V_1 = V_{DD}$

where

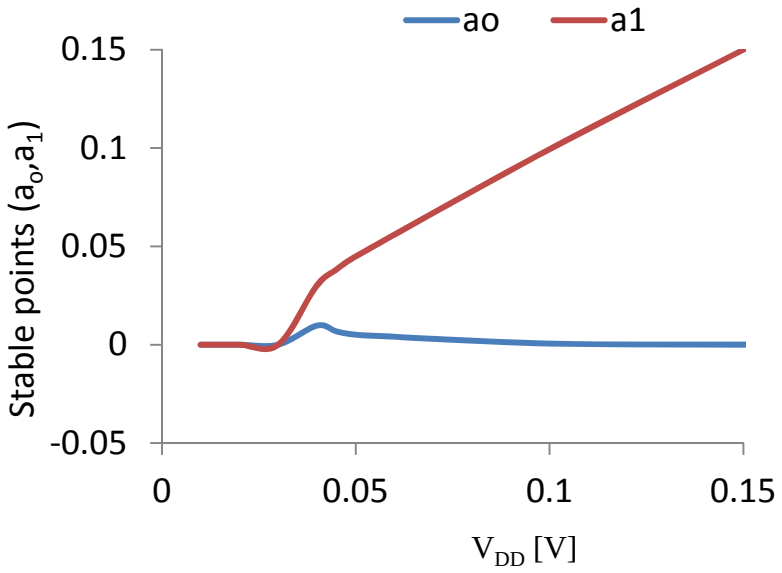
$$a_o = \frac{b}{2}\left(b - \sqrt{b^2 - 4}\right) \qquad b \equiv \exp\left(\frac{V_{DD}/2}{U}\right)$$

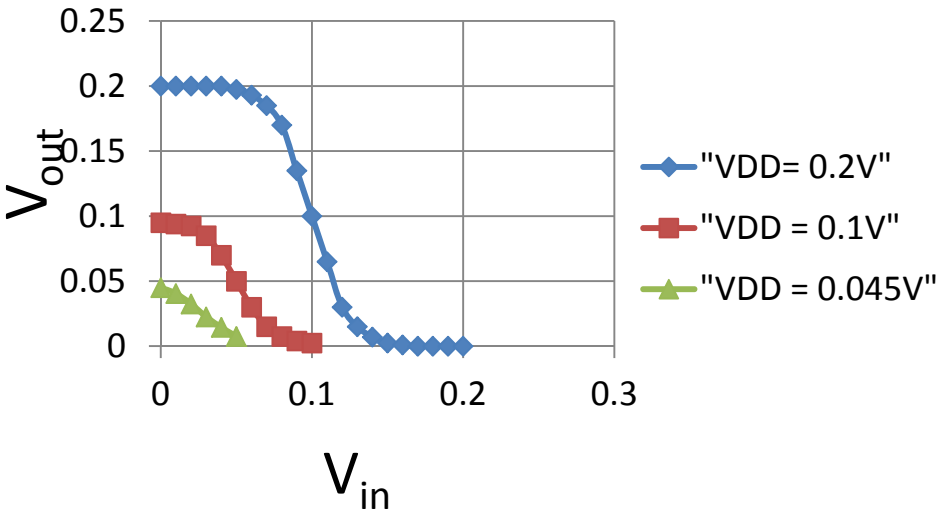
$$a_1 = \frac{b}{2}\left(b + \sqrt{b^2 - 4}\right)$$

U = thermal voltage (~26mV)



The minimum VDD is the point when the logical states lose their distinguishability.





$$a_o = a_1$$

$$a_o = \frac{b}{2}\left(b - \sqrt{b^2 - 4}\right)$$

$$a_1 = \frac{b}{2}\left(b + \sqrt{b^2 - 4}\right)$$

$$\frac{b}{2}\left(b - \sqrt{b^2 - 4}\right) = \frac{b}{2}\left(b + \sqrt{b^2 - 4}\right)$$

$$\sqrt{b^2 - 4} = 0$$

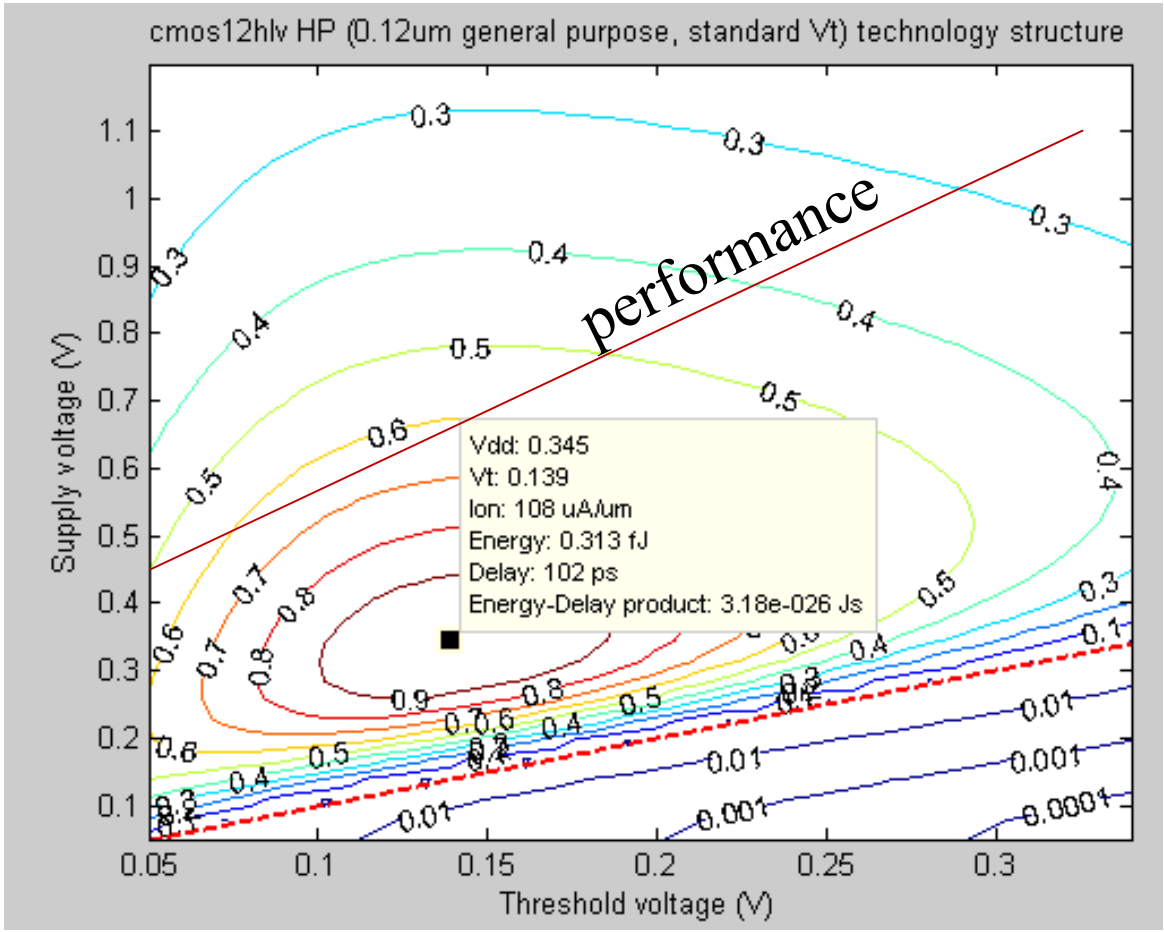
$$\therefore b = 2$$

$$b \equiv \exp\left(\frac{V_{DD}/2}{U}\right)$$

$$\rightarrow V_{DD} = 2U\ln(2)$$

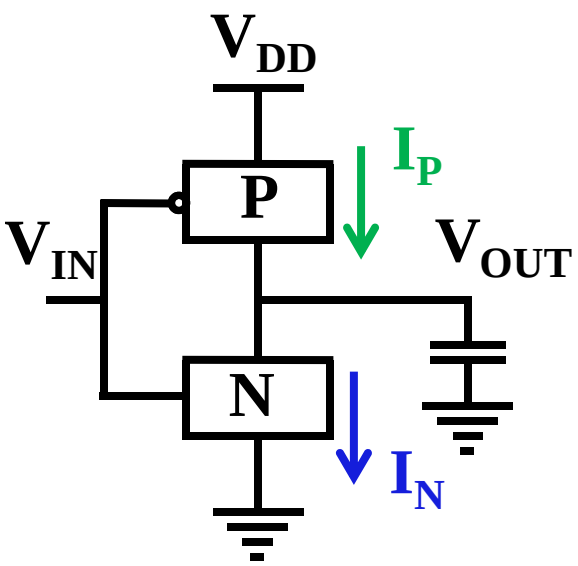
$$\rightarrow \mathrm{V_{DD}} = 0.036\mathrm{V}$$

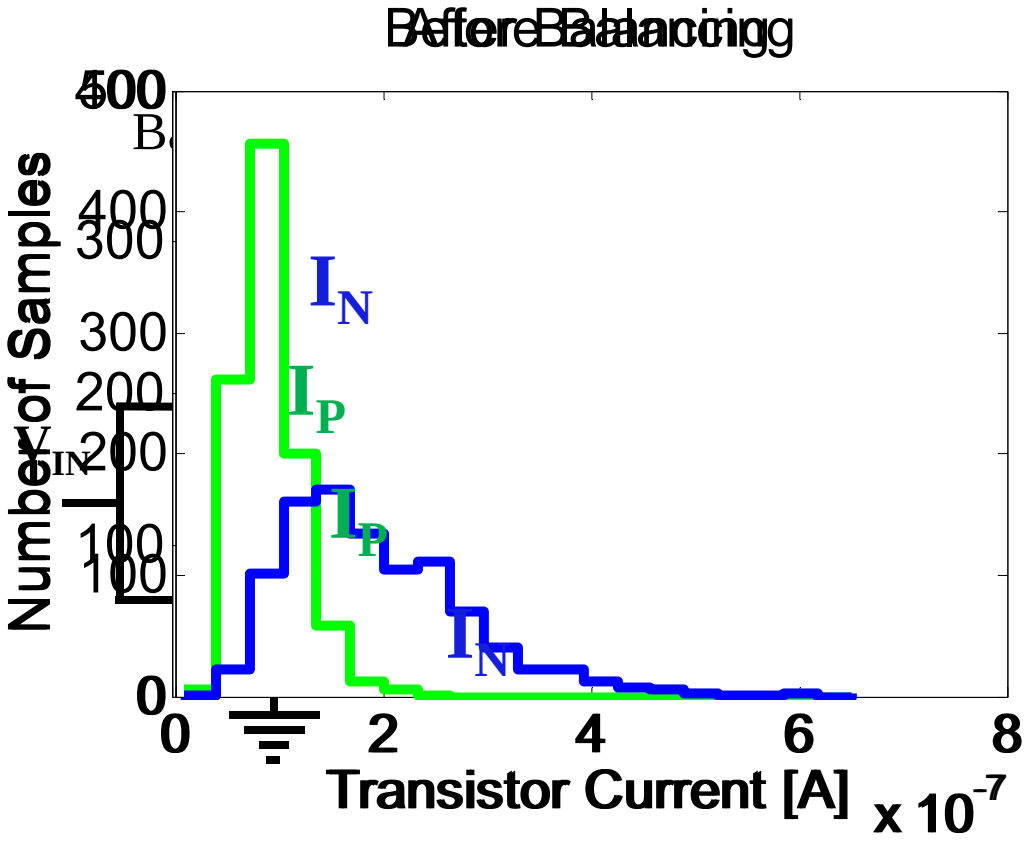
Energy Contour Plots



- Same performance but at distinct energy levels
  - Choice of VDD and Vt

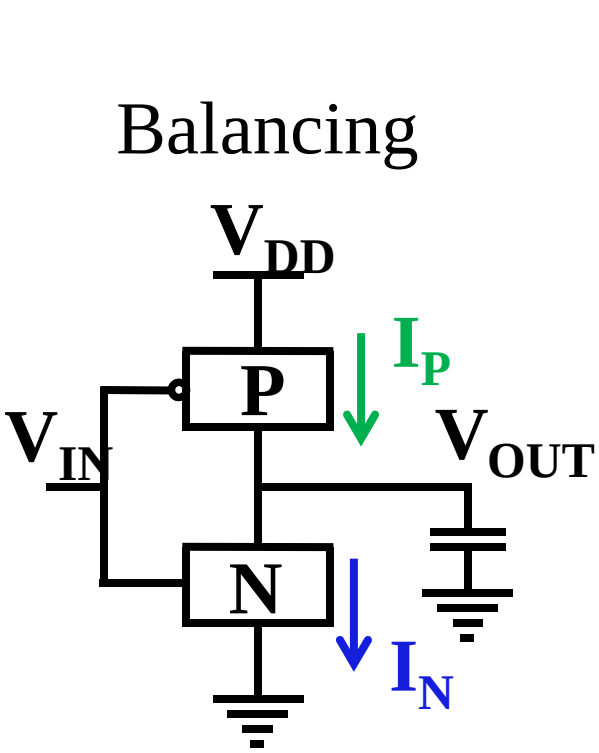
Std. Cell Library Design for SubVT

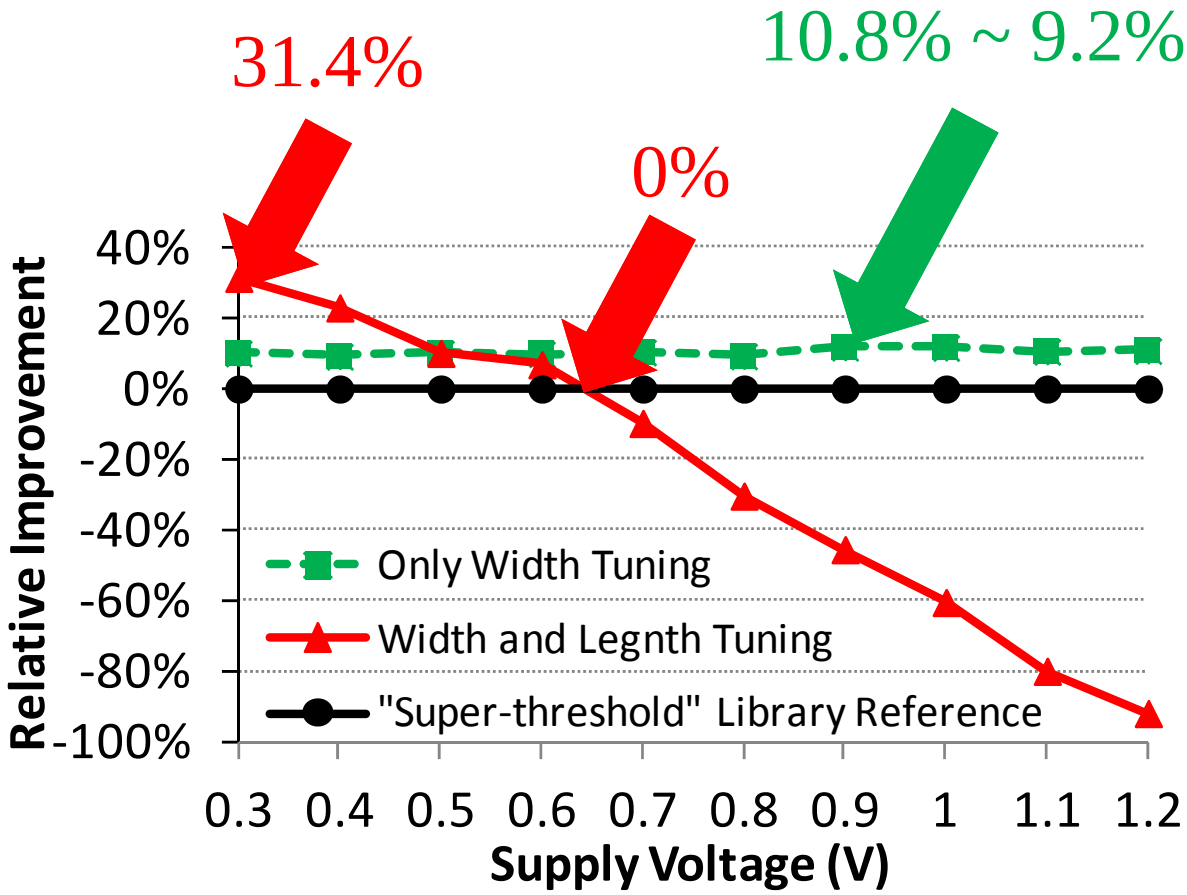




$$E[I_n] = E[I_p] \Rightarrow \frac{W_n L_p}{W_p L_n} = \alpha e^{\frac{E[V_{thn}] - E[V_{thp}]}{nU}} e^{\frac{Std^2[V_{thp}] - Std^2[V_{thn}]}{2(nU)^2}}$$

Std. Cell Library Design for SubVT





LV Designs

Multi-Resource Architecture

Constant Throughput

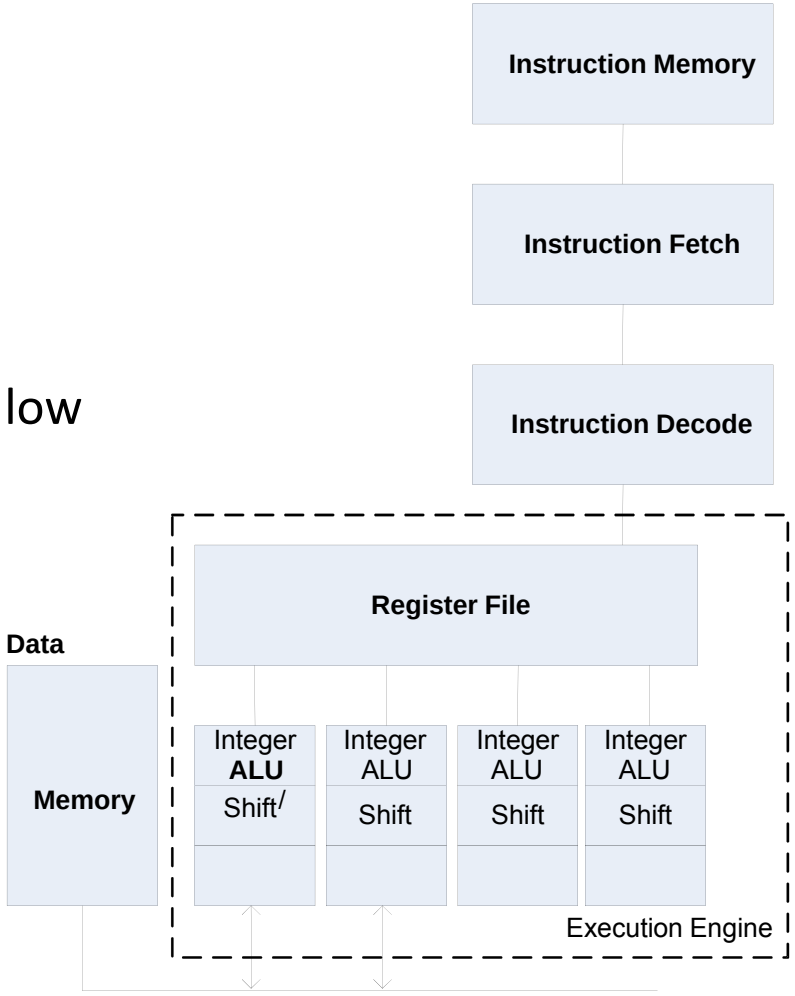
- Constant throughput
- Full program parallelization
- Use FBB to trade-off area/speed
- Time multiplexing circuit overhead
- Static power consumption dominates at low voltage

$$\frac{P_{VddN}}{P_{Vdd1}} = [N + \lambda(N-1)]\frac{V_{ddN}^{\ 2}}{V_{dd1}^{\ 2}}[1 - p + \frac{p}{N}]$$

Processors

Processor Overhead

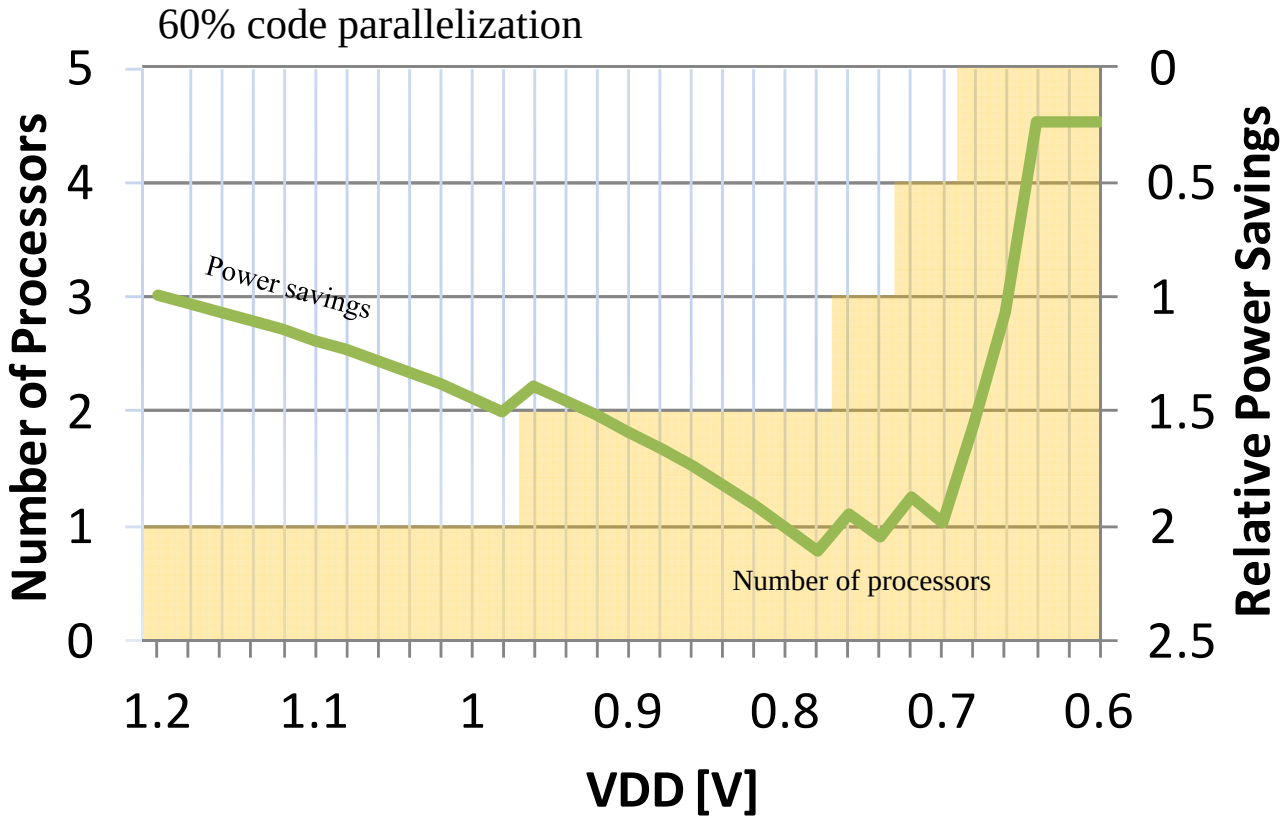
Portion of parallelizable programming code



LV Multi-Resource Platform

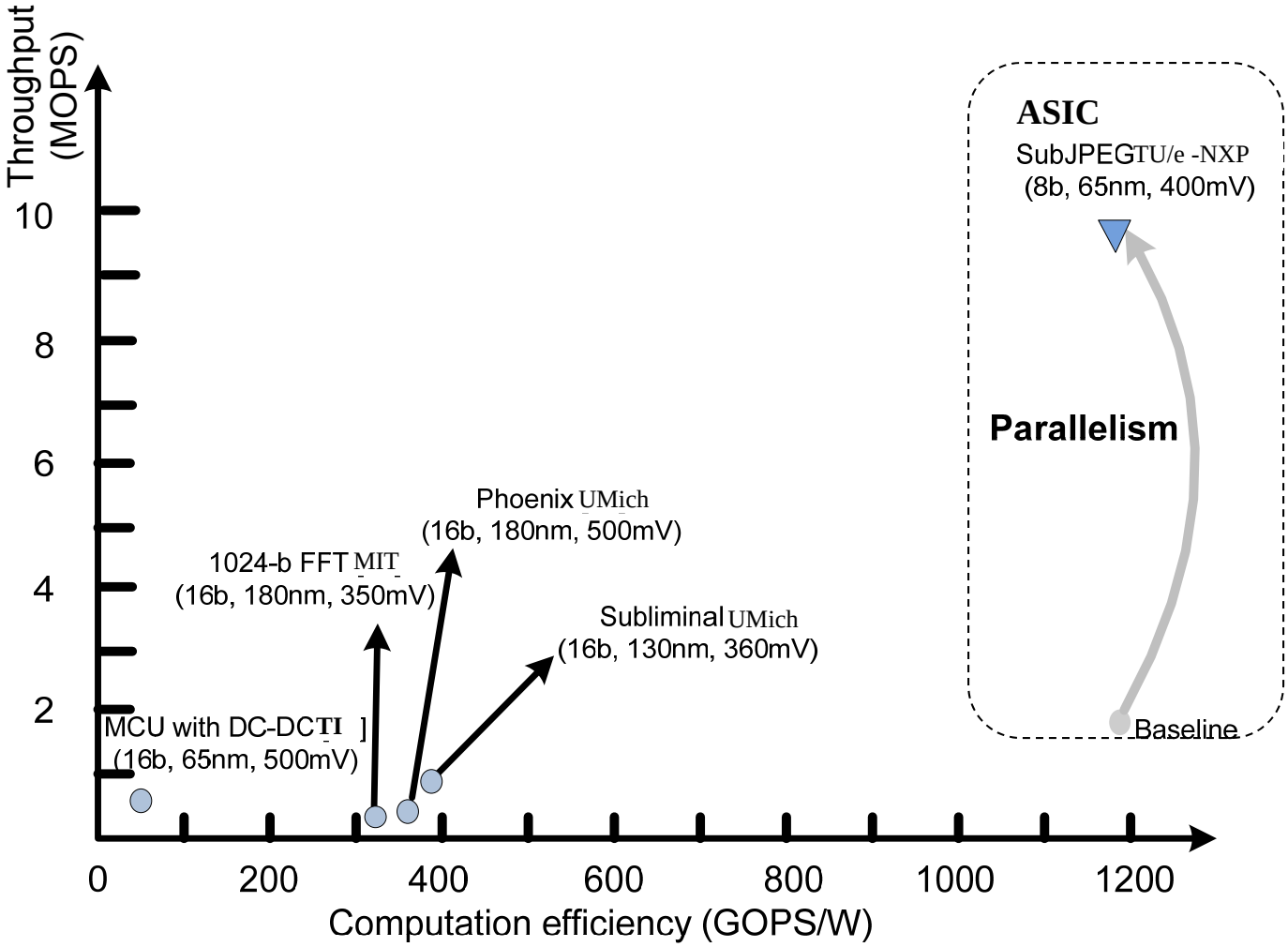
Optimization of number of resources

Constant Throughput



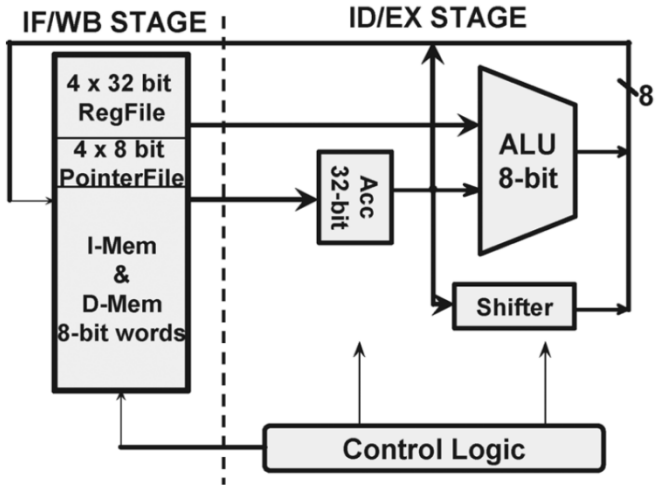
- Based on Amdahl's Law to account for amount of parallelism in programming code

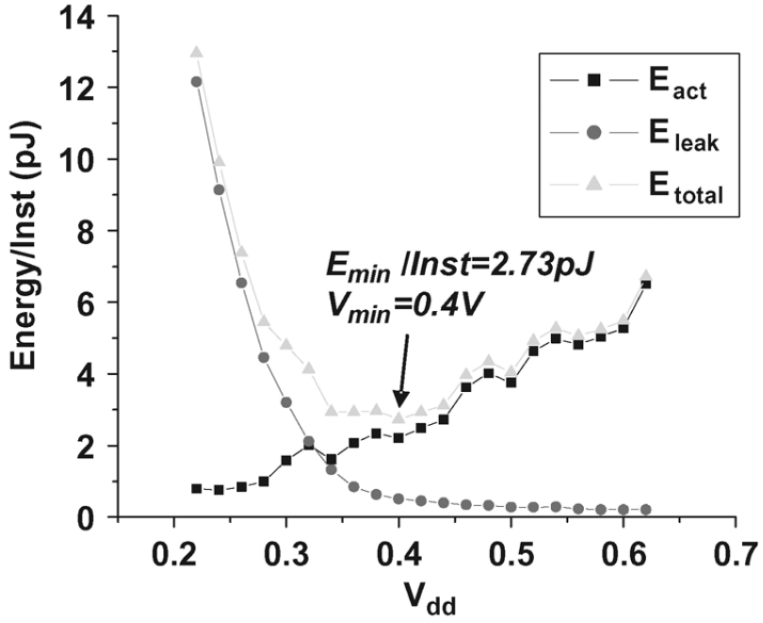
Subthreshold Processors



Minimum Energy Microprocessor

Bo Zhai, Sanjay Pant, Leyla Nazhandali, Scott Hanson, Javin Olson, Anna Reeves, Michael Minuth, Ryan Helfand, Todd Austin, Dennis Sylvester, and David Blaauw
Energy-Efficient Subthreshold Processor Design
IEEE Transactions On Very Large Scale Integration Systems, Vol. 17, No. 8, August 2009



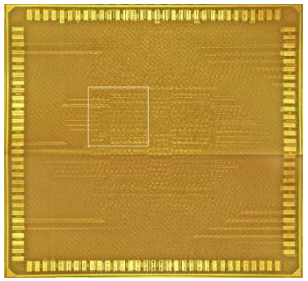


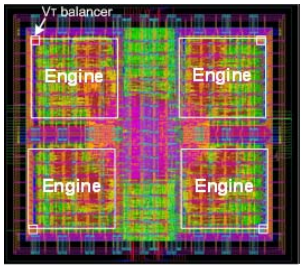
- Distinct architecture strategy for subthreshold
  - 2-stage pipeline, custom memory
- Subliminal Processor
  - CMOS 130nm
  - VDDmin = 200mV
  - 2.6pJ/instruction @ 360mV, 833KHz

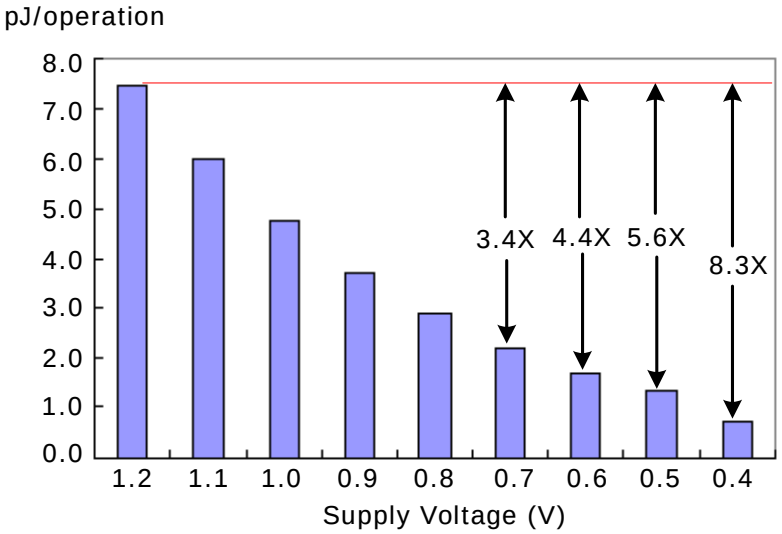
Ultra Low-Power Design

Low Energy Systems for Consumer Electronics (JPEG encoder)

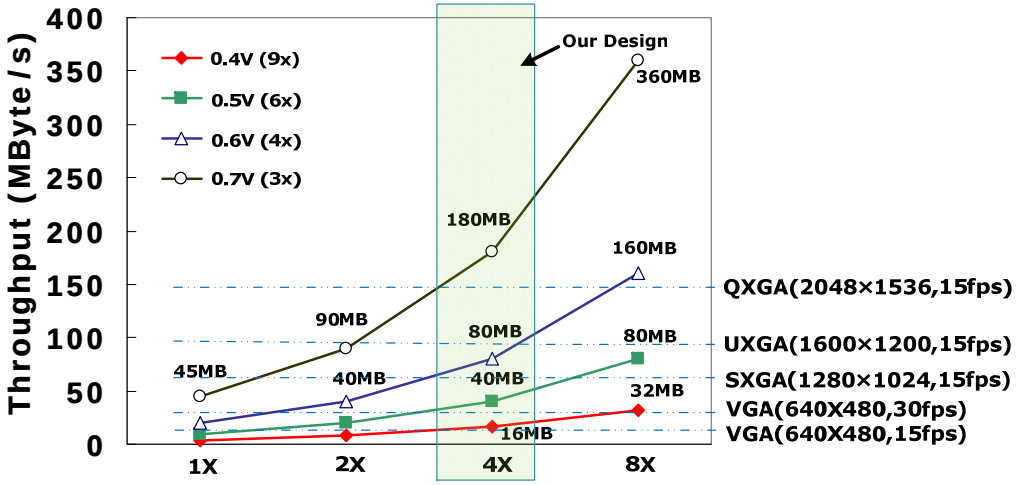
1. Optimum operating conditions
   - Wide-VDD operating range:
     From subthreshold to super threshold
   - Multiple clock domains
   - Performance compensation due to process variability
2. High Throughput at Low Energy
   - System partitioning for low-voltage operation and massive parallelism







Energy/Operation



Possible real-time image applications

One cannot think that in a few years, without power management, any kind of competitive chip can be marketed in the entire application field.

No computing device, from chips in hearing aids all the way to massively parallel computer clusters will be allowed to waste power.