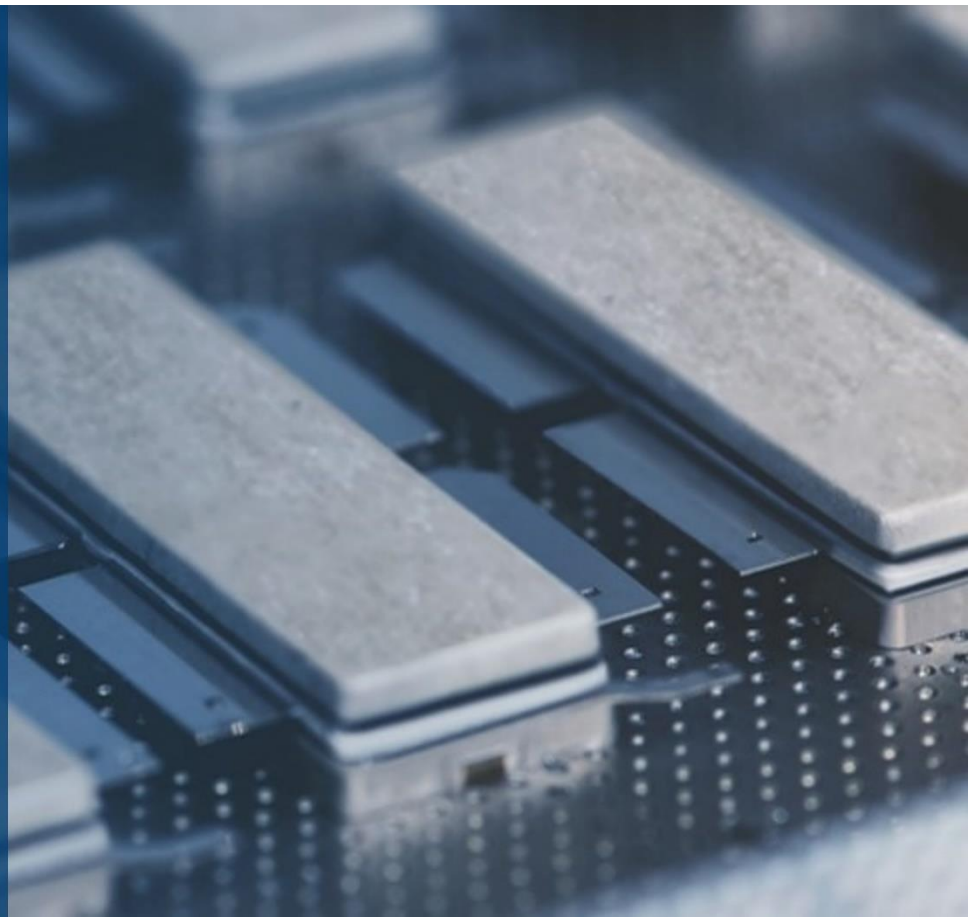


Sept 15, 2023

# Next generation of efficient 6G power amplifiers

Fred van Rijs

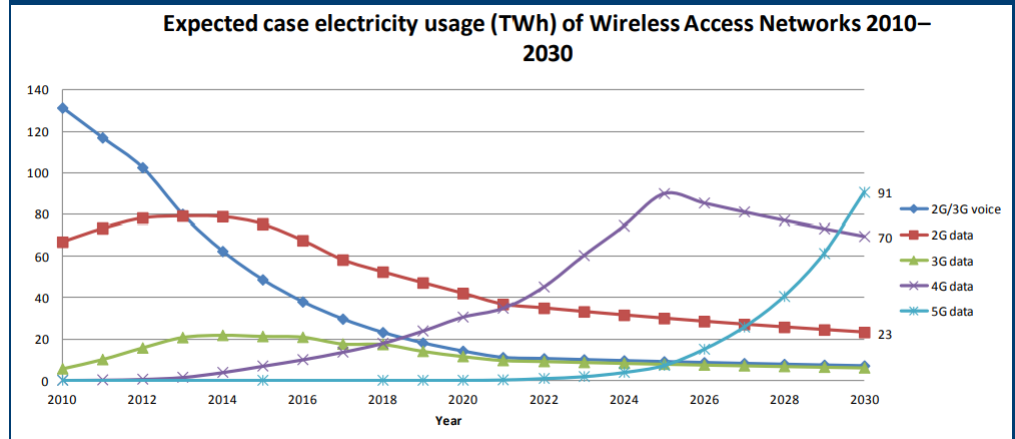
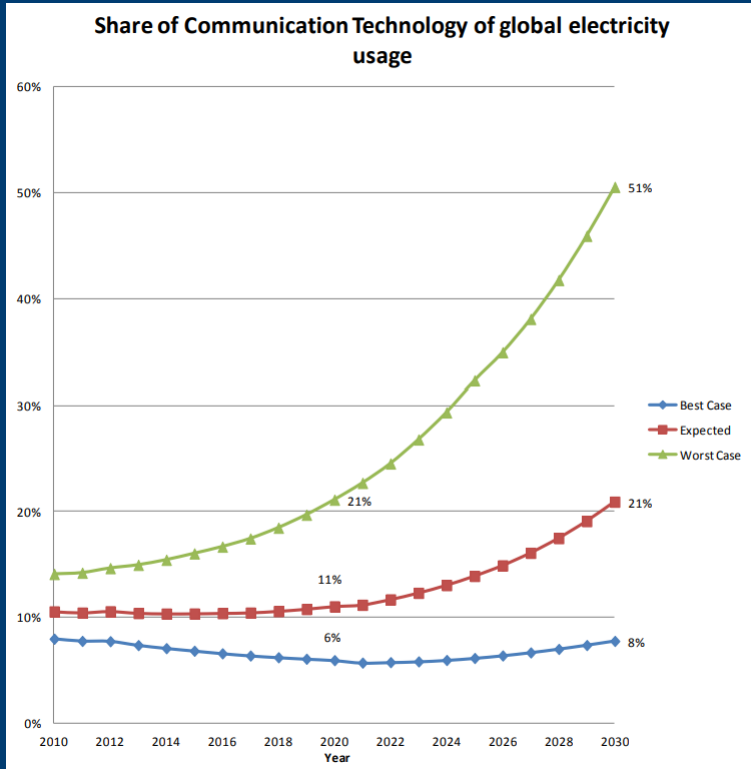


# Content

- The need for energy/power efficiency
- Overview current BST systems
  - Technology trends
  - PA concepts
- State of the art PA efficiencies
- Summary

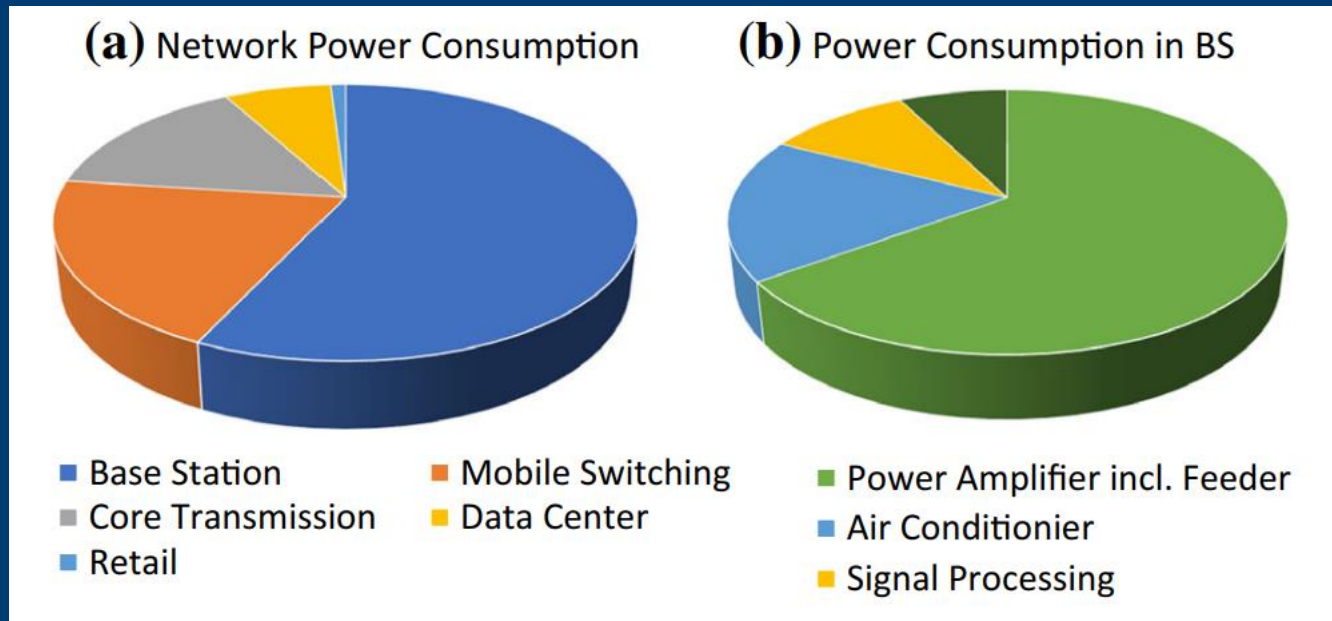
# The need for energy/power efficiency

- Telecommunication infrastructure accounts now for 2-3% of total global energy consumption.
- Data efficiency is increasing (bits/Joule) but with increasing data capacity targets of 5/6G the number of basestation increases more rapidly.
- This could lead to 20% of global energy consumption of CT in 2030.



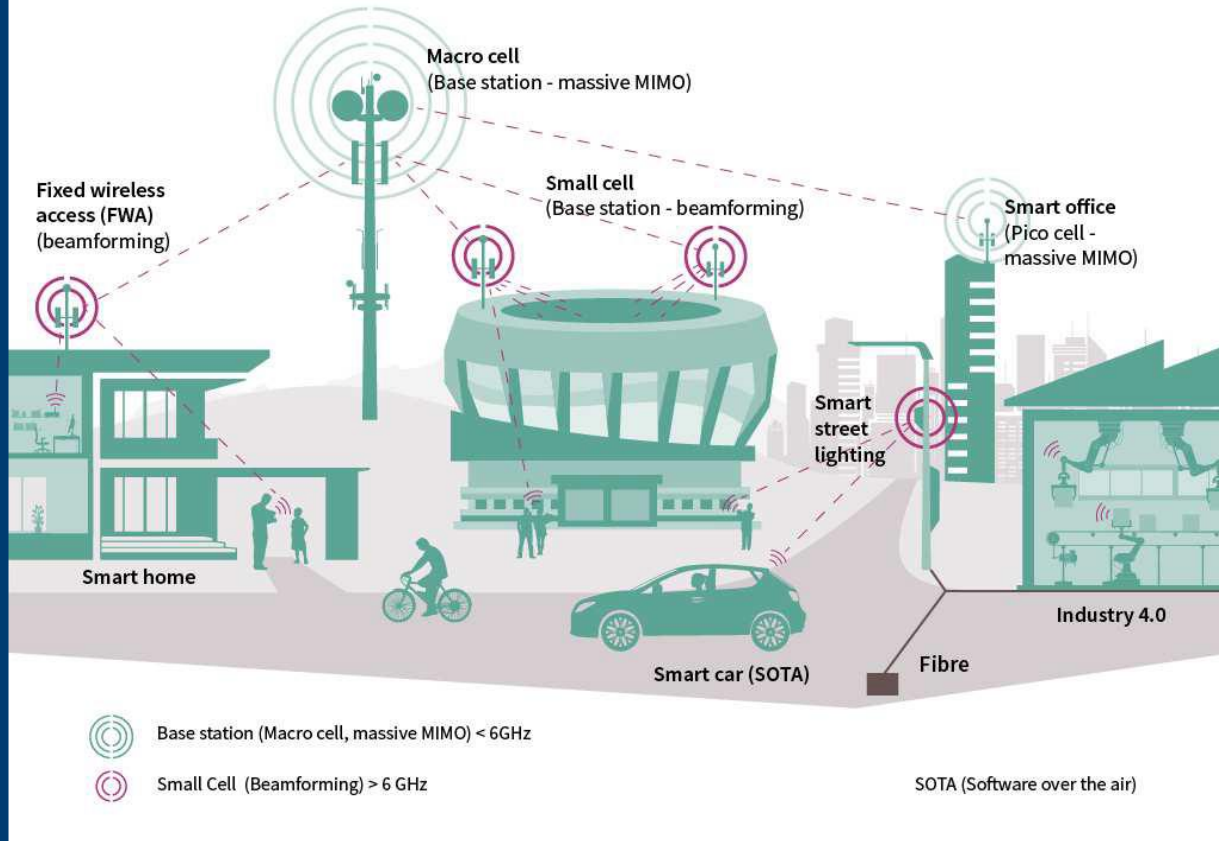
# The need for energy/power efficiency

- Power amplifier is one of the main contributors to total BST power consumption.



From white paper Ericsson

## Smart and connected - the communication of tomorrow with 5G

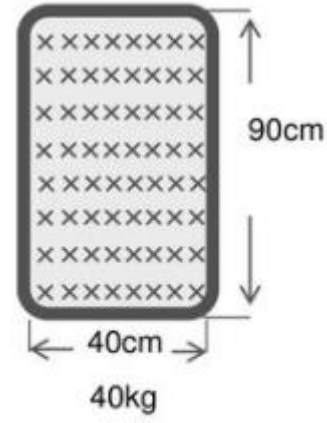


## Current systems from PA perspective.

### Sub 6GHz systems:

- Macro BST:
  - Psat 300-1000 W
- mMIMO:
  - Psat: 30-100 W
- Small cells:
  - Psat: < 10 W





Massive MIMO  
Antenna geometry  
(3300-4200 MHz)



# Currently



## Typical modern 4/5G macro base station amplifier:

600 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1930 MHz to 1995 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$  in an asymmetrical Doherty production test circuit.  $V_{DS} = 30\text{ V}$ ;  $I_{Dq} = 1060\text{ mA}$  (main);  $V_{GS(amp)peak} = 1.0\text{ V}$ , unless otherwise specified.

Test signal	f (MHz)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR (dBc)
1-carrier W-CDMA	1930 to 1995	30	112	15.5	48.5	-34 <a href="#">[1]</a>

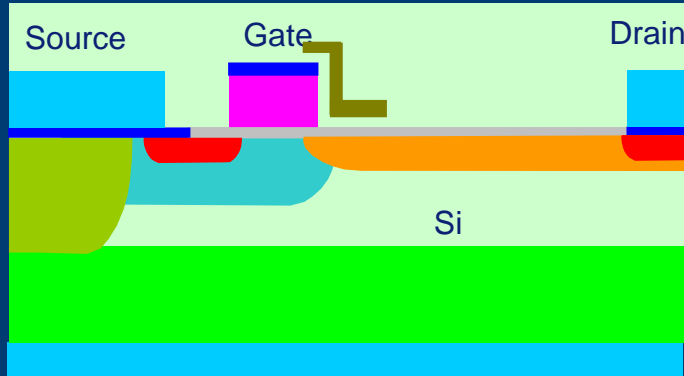
## Main-stream technologies:

1. LDMOS and GaN semiconductor technology
2. Doherty PA concept

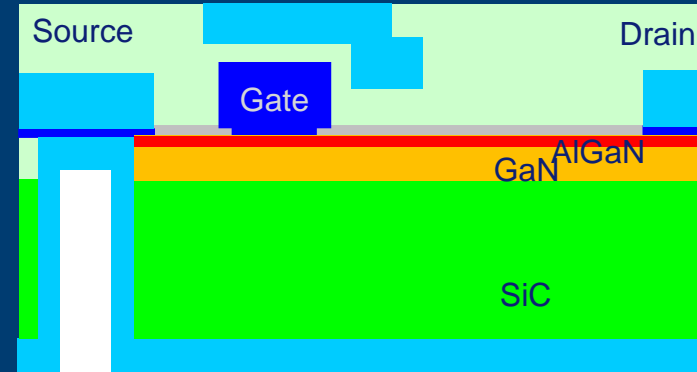


# Device technologies

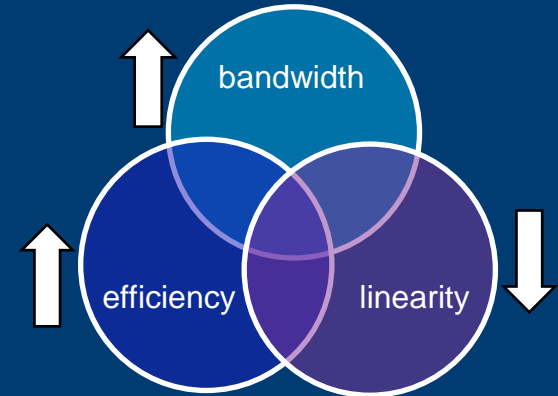
## LDMOS



## GaN-HEMT



	Si-LDMOS	GaN HEMT
Supply voltage ( $V_{dd}$ )	30 V	50 V
Power-density ( $P_{dens}$ )	1.5 W/mm	9 W/mm
Peak Efficiency	70%	80%
Output capacitance ( $C_{ds}$ )	0.18 pF/W	0.04 pF/W
RF Bandwidth FOM ( $\propto \frac{1}{V_{dd}^2 C_{ds}}$ )	1	1.6

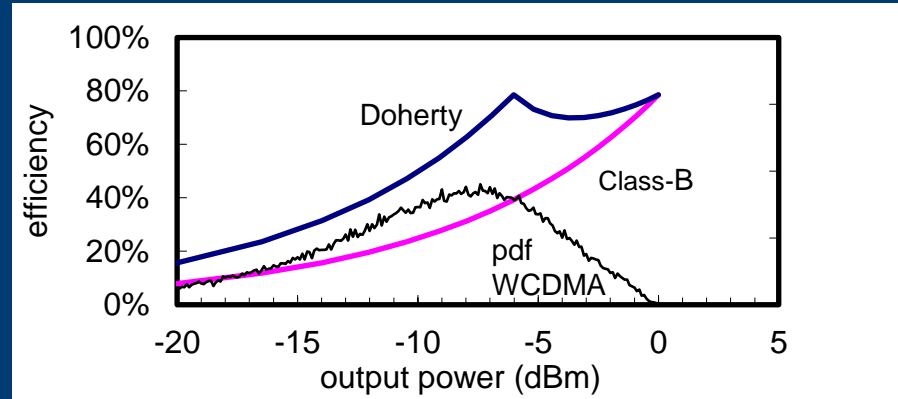
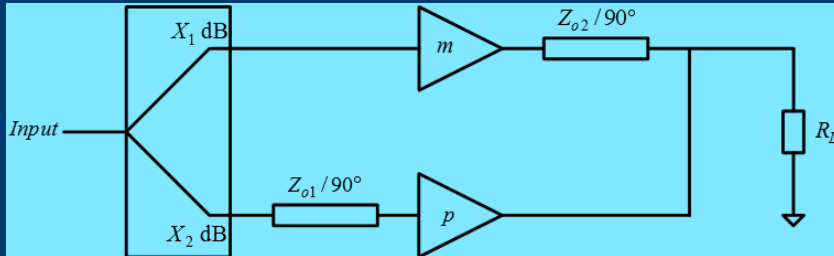




# Doherty PA concept.

Doherty PA to increase efficiency in back-off. Essential for modulated signals.

W. H. Doherty, "A new high efficiency power amplifier for modulated waves", *Proc. IRE*, vol. 24, no. 9, pp. 1163-1182, 1936.



Theoretically, with peak efficiency of 78% and 8dB PAR:

- The average efficiency in class-B: 35%
- With Doherty concept (asym) : 60%

In practice, with new requirements, the limits of Doherty becomes visible.

# Interesting new PA concepts

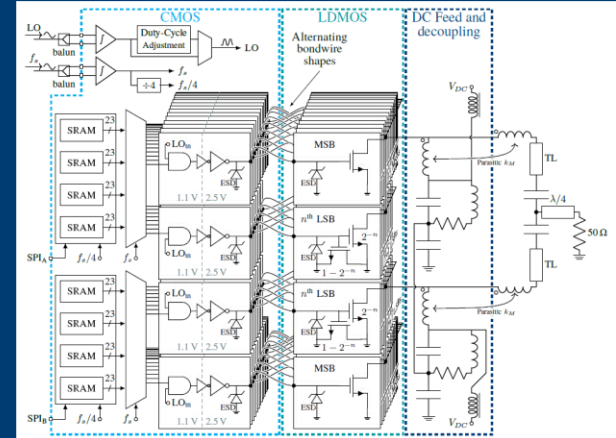
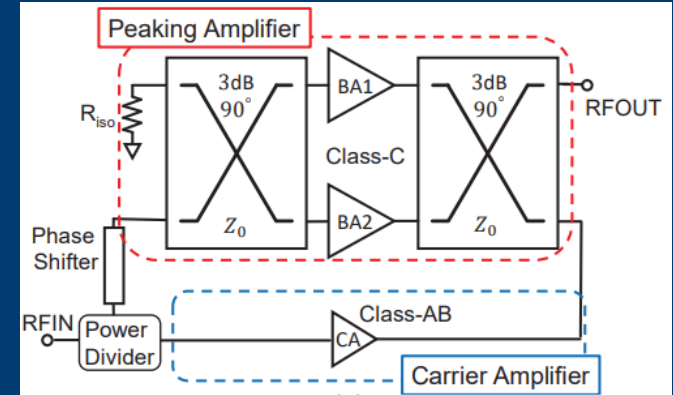
Two approaches:

(1) Combinations of existing concepts e.g.

- Doherty-Chireix concept
- Doherty-voltage modulation concept
- Load modulated balanced PA
- ...

(2) Digital intensive PA's (RF-DAC)

Tudelft,  
IMS2020, R.J. Bootsman, et al.  
“An 18.5 W fully-Digital Transmitter with  
60.4% Peak System Efficiency.”



# Efficiency trade-offs

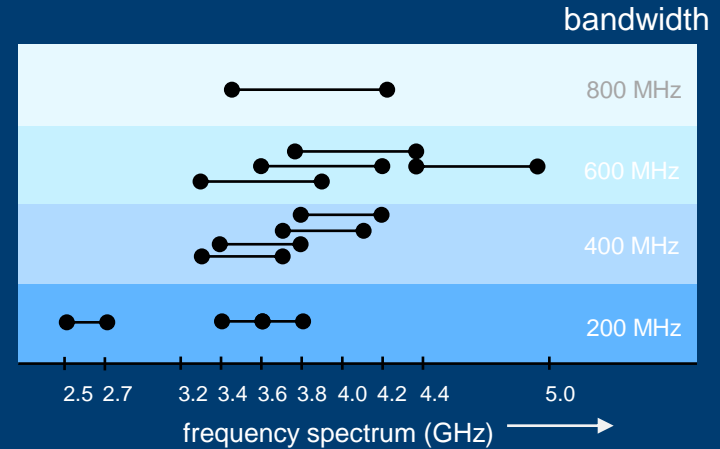
$$\eta_{LU} = \eta_{peak} \eta_{mod} \eta_{driver} \eta_{iso}$$

$\eta_{peak}$ : peak efficiency	LDMOS: 0.7 GaN: 0.8
$\eta_{mod}$ : average efficiency	Class-AB: 0.4 Doherty: 0.7
$\eta_{driver}$ : including drivers	Typical: 0.95
$\eta_{iso}$ : isolator losses	Typical: 0.93
$\eta_{LU}$ : total LU efficiency	Typical: 0.5



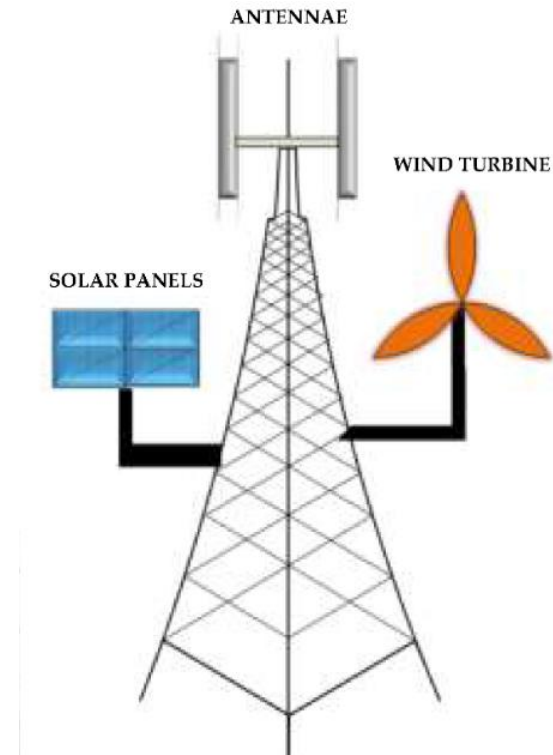
# Massive MIMO system trends on PA-level

- Per PA less output power is required.
- Move to higher frequencies
- Much larger bandwidth required
- More digital pre-distortion friendly: linearity

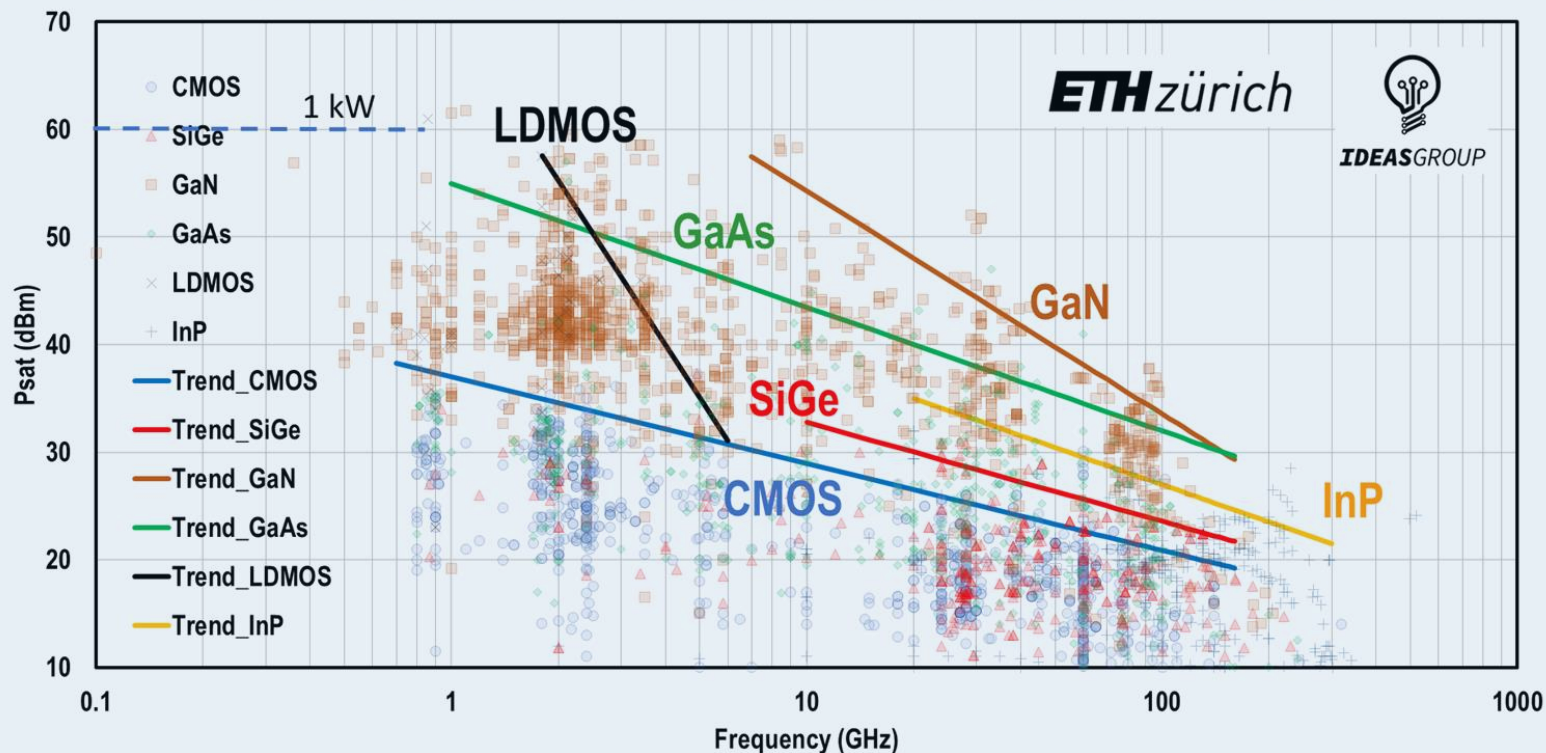


iBW	100 MHz	200 MHz	400 MHz	400 MHz	600 MHz	800 MHz
#T/total Pout	120 W	240 W	320 W	400 W	600 W	640 W
32T		7.5/75	10/100	12.5/125	18.7/187	20/200
64T	1.9/19	3.8/38	5/50	6.3/63	9.4/94	10/100
128T					4.7/47	5/50
256T						2.5/25

# State of art PA efficiencies



## PA Survey Version 8: Saturated Output Power vs. Frequency (All Technologies)

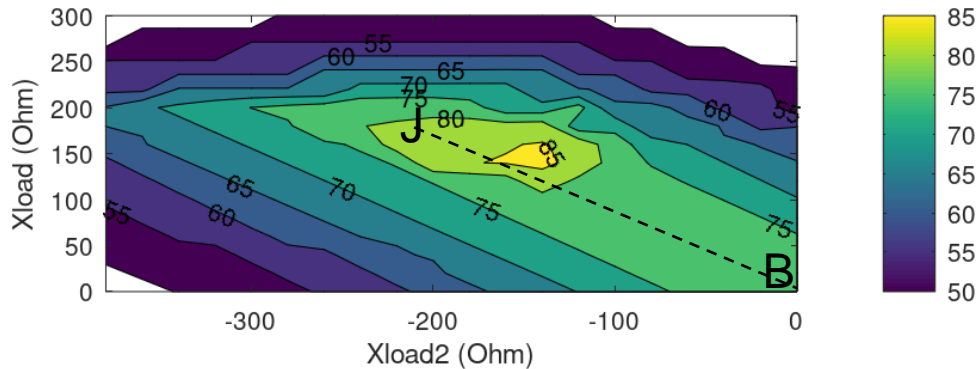


- Technologies needed depends very much on required power levels (from ETH PA Survey).

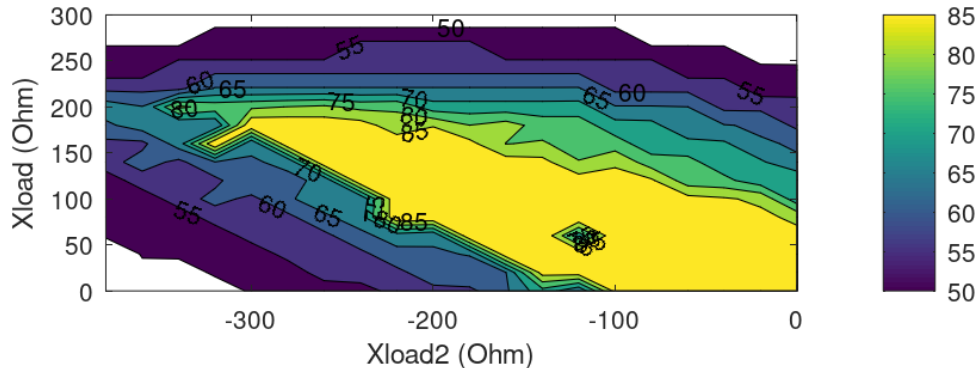


# Theoretical efficiency limit

Max efficiency: second harmonic



Max efficiency: with third harmonic



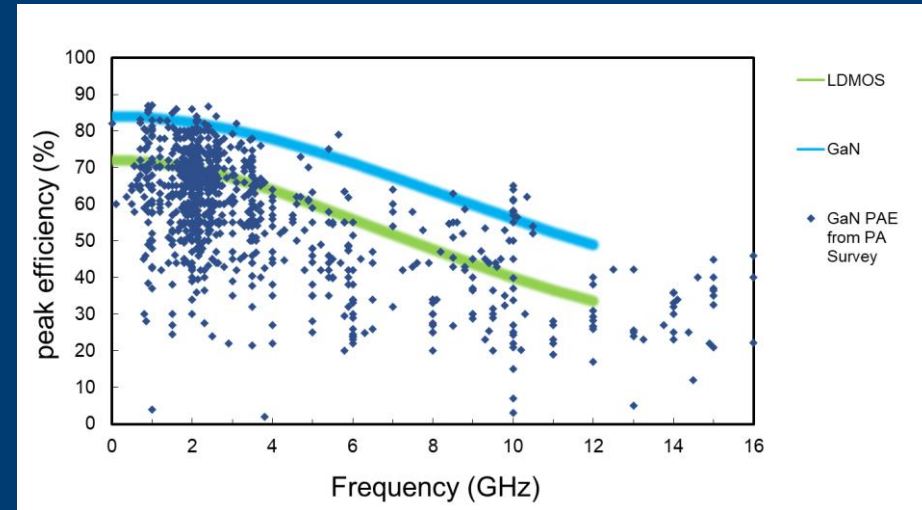
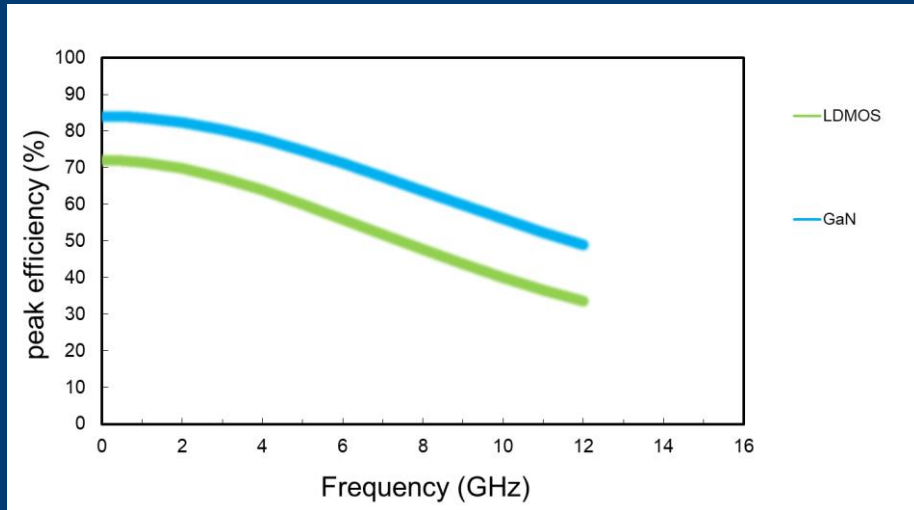
Max obtainable efficiency for ideal transistor with real IV-curves.

n	Efficiency	class
1	78%	B
2	85%	J
3	90%	

Table from F. Raab.

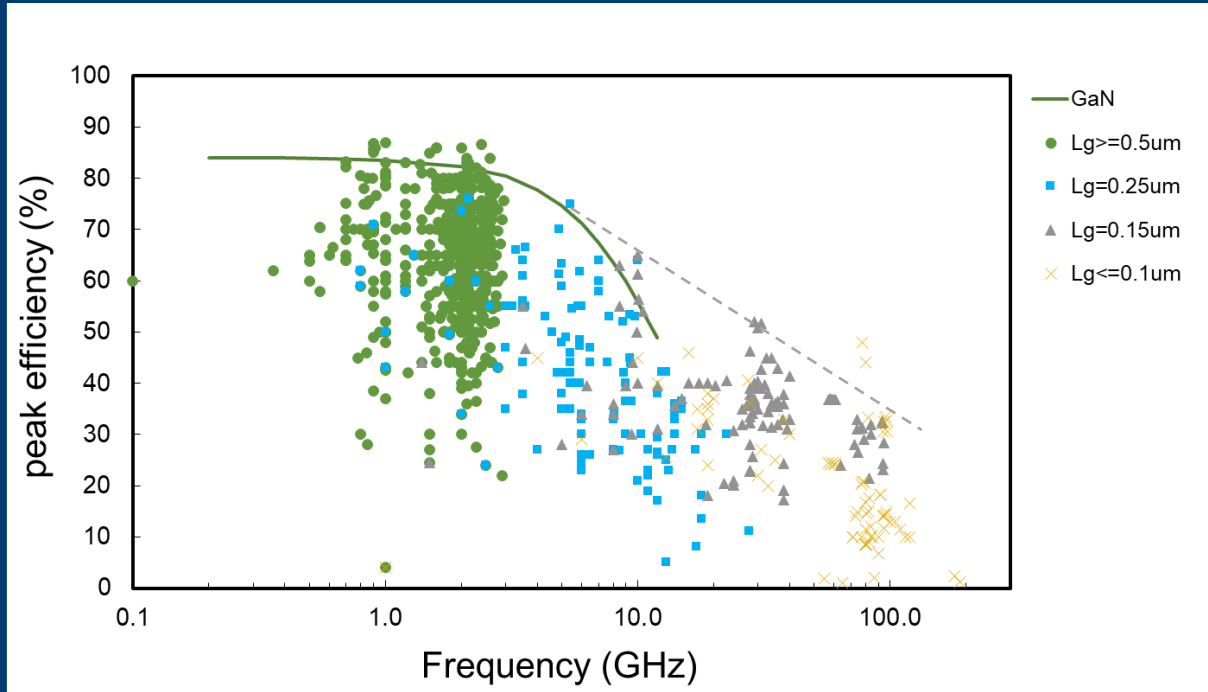
m	n = 1	n = 3	$\eta$	n = 5	n = $\infty$
1	$1/2 = 0.500$	$1/3^{1/2} = 0.5774$		0.6033	$2/\pi = 0.637$
2	0.7071	0.8165		0.8532	0.9003
4	0.7497	0.8656		0.9045	0.9545
$\infty$	$\pi/4 = 0.785$	0.9069		0.9477	1 = 1.000

# Efficiency performance vs frequency



- Slow decline of efficiency vs frequency (left).
- Results confirmed by data from literature (right).

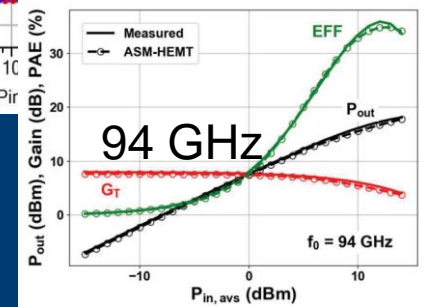
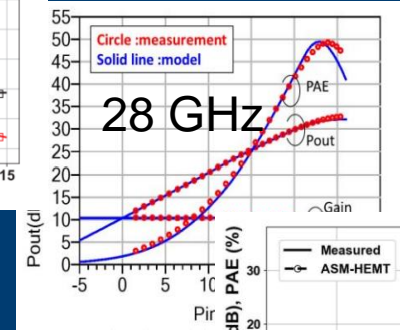
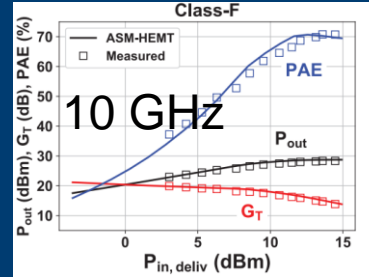
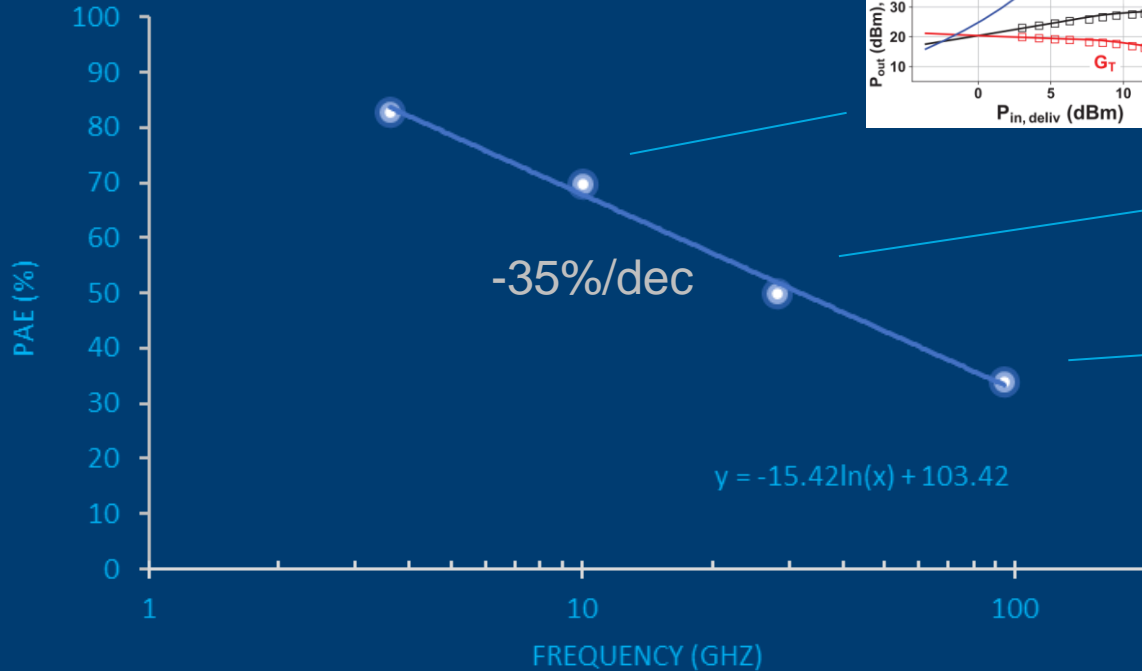
# Efficiency performance extended to THz frequencies for GaN



- There seems to be a universal curve

# Best efficiency performance vs frequency

$$\eta_{LU} = \eta_{peak} \eta_{mod} \eta_{driver} \eta_{iso}$$



# Summary: The need for energy/power efficiency

$$\eta_{LU} = \eta_{peak} \eta_{mod} \eta_{driver} \eta_{iso}$$

	Sub 6 GHz	94 GHz
$\eta_{peak}$ : peak efficiency	GaN: 0.8	0.3 (other technologies?)
$\eta_{mod}$ : average efficiency	Doherty: 0.7	? (class AB)
$\eta_{driver}$ : including drivers	Typical: 0.95	↓ (need more gain/stage)
$\eta_{iso}$ : isolator losses	Typical: 0.93	↓ (balun)
$\eta_{LU}$ : total efficiency	Typical: 0.5	Typical: 0.10 (peak eff)

- Surely, the PA efficiency can never reach efficiencies of sub 6GHz. But much can also be done at system level.

A close-up, blue-tinted photograph of a microchip or integrated circuit. The chip's surface is covered with intricate patterns of metal and silicon, including various rectangular pads, lines, and a grid of small circular features. The lighting creates a sense of depth and highlights the fine details of the technology.

It is clear that advances need to be made at all levels.

Thanks for your attention.